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# APPLICATION NOTE 5602 In-System Programming Using I2C Bootloader Commands

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Abstract: This application note describes I<sup>2</sup>C bootloader commands supported by optical microcontrollers. The bootloader commands are executed from functions in the utility ROM (UROM). The application note specifies the I<sup>2</sup>C master and I<sup>2</sup>C slave command response protocol, which interacts with the I<sup>2</sup>C slave to execute the bootloader commands. It also describes various methods of in-system programming (ISP) using the I<sup>2</sup>C slave bootloader commands.

# Introduction

The DS4830 has a program segment known as utility ROM (UROM), which provides various system utility functions. This allows in-system programming (ISP) using the I<sup>2</sup>C slave interface. The DS4830 reset vector is located in the utility ROM at address 8000h. Following each poweron reset (POR), the DS4830 automatically starts execution from the utility ROM, which allows the ROM code to perform any necessary system support functions.

The utility ROM provides the following utility functions.

- Reset vector
- Bootstrap function for system initialization
- In-circuit debug
- ISP using JTAG or I<sup>2</sup>C slave interface

# In-System Programming Using the I<sup>2</sup>C Bootloader

The DS4830 has a special bit, I2C\_SPE, which does not change on I<sup>2</sup>C soft reset or external reset. This bit is used to identify the I<sup>2</sup>C bootloader function. The I2C\_SPE bit is not writable in the application program; this bit can be written through UROM code only. The DS4830 has the dedicated slave address 34h, which is always visible on the active I<sup>2</sup>C slave interface and cannot be disabled without disabling the I<sup>2</sup>C slave interface. Slave address 34h is used to communicate directly with the UROM code. When the slave address 34h receives the Enter I<sup>2</sup>C Bootloader command, it sets the I2C\_SPE bit. On reset, the UROM code checks the I2C\_SPE bit. If I2C\_SPE is clear, code execution jumps to the flash location 0000h in the application program. Otherwise, execution remains in UROM to execute utility functions. For more information, see the In-System Programming section in the user guide 5484, "DS4830 Optical Microcontroller User's Guide."

Table 1. P	<sup>2</sup> C Bootloader C		Password
Family	Command	Command Description	Protected
	00h	No Operation	Ν
	01h	Exit Loader. With this command, the bootloader exits, clears the JTAG_SPE and I2C_SPE bits, and performs an internal reset.	Ν
	02h	Master Erase. This command erases (sets to FFFFh) the words in the program flash memory, writes (sets to 0000h) all words in the data SRAM, and clears the password lock bit.	Ν
	03h	Password Match. This command matches the 32-byte password value to that in program memory to clear the password lock bit.	Ν
0	04h	Get Status. This command monitors the bootloader Status Flags and Status Code.	Ν
	05h	Get Supported commands	Ν
	06h	Get Code Size	Ν
	07h	Get Data Size	Ν
	08h	Get Loader Version	Ν
	09h	Get Utility ROM Version	Ν
	0Dh	ID Banner command	Ν
1	10h	Load Code. This command programs data into the program flash memory.	Υ
I	11h	Load Data. This command programs data into the SRAM.	Υ
2	20h	Dump Code. This command reads data from the program flash memory.	Υ
2	21h	Dump Data. This command reads data from the SRAM.	Υ
3	30h	CRC Code. This command calculates the CRC of the program flash memory.	Υ
3	31h	CRC Data. This command calculates the CRC of the SRAM.	Υ
4	40h	Verify Code. This command verifies that the data written in the program flash memory matches the input data with this command.	Υ
-	41h	Verify Data. This command verifies that the data written in the SRAM matches the input data with this command.	Y
5	50h	Load and Verify Code. This command programs data into the program flash memory and verifies the data immediately after each word.	Υ
J	51h	Load and Verify Data. This command programs data into the SRAM and verifies the data immediately after each word.	Υ
E	E0h	Code (Flash) Page Erase	Y

The utility ROM provides the following functions for ISP using the I<sup>2</sup>C slave interface.

1. Enter I<sup>2</sup>C bootloader

2. Poll 3Eh

- 3. Master Erase command
- 4. Flash programming commands
  - a. Load and Verify Code command (50h)
  - b. Load Code command (10h) and Verify Code command (40h) (alternate method)
  - c. Load Code command (10h) and Dump Code command (20h) (alternate method)
- 5. Get Status command
- 6. Exit Bootloader command

See Figure 1 for ISP.

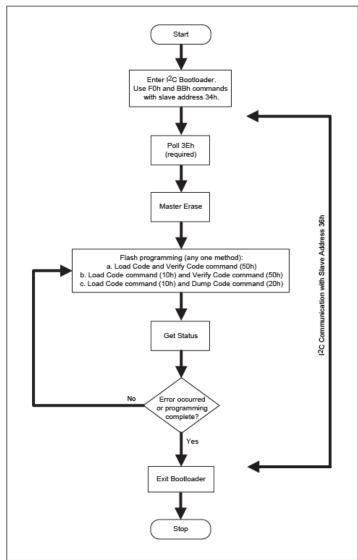


Figure 1. Flowchart of flash ISP.

See Figure 2 for the colors used to differentiate the I<sup>2</sup>C master sequence/response, the bootloader command, and the bootloader (I<sup>2</sup>C slave) response.

I <sup>2</sup> C Master Sequence/Response
Bootloader Command Send by the I <sup>2</sup> C Master
Bootloader (I <sup>2</sup> C Slave) Response

Figure 2. I<sup>2</sup>C master-slave communication color indicators for the bootloader commands.

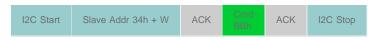
#### 1. Enter I<sup>2</sup>C Bootloader

The DS4830 has the dedicated slave address 34h, which is always visible on the DS4830 active I<sup>2</sup>C slave interface. This slave address is used to enter bootloader mode from the application. To enter bootloader mode, the I<sup>2</sup>C communication sequence should be as follows.

a. Set the I2C\_SPE bit by sending command F0h as shown below.



b. Reset the device by either using the I<sup>2</sup>C reset command BBh (with slave address 34h) or by toggling the active-low RST pin.



# 2. Poll 3Eh

The UROM acknowledges the execution of commands by sending 3Eh after the execution of every command. This polling for 3Eh at the end of every command execution is required for the correct functioning of the UROM functions.

## Polling 3Eh for I<sup>2</sup>C bootloader Read

The I<sup>2</sup>C Read command operation can be terminated by reading an additional byte. The additional byte should be 3Eh. For example, the Get Status command provides two bytes of status. To terminate this command, the I<sup>2</sup>C master should read three bytes and send NACK to the last byte. See **Figure 3** for the I<sup>2</sup>C bootloader Read operation.

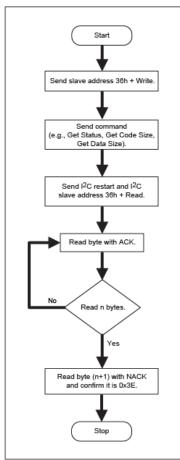


Figure 3. I<sup>2</sup>C bootloader Read operation.

# Polling 3Eh for I<sup>2</sup>C bootloader Write

The completion of the execution of the UROM I<sup>2</sup>C Write command operation can be identified by polling 3Eh after the I<sup>2</sup>C Write operation. See **Figure 4** for 3Eh polling after the Write command operation. The Exit Bootloader command is an exception that does not require 3Eh.

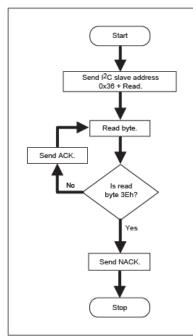


Figure 4. I<sup>2</sup>C bootloader Write operation.

Either of the following two sequences can be used to poll for 3Eh after a Write command operation.

#### Method 1

In this method, the I<sup>2</sup>C master starts reading data from slave address 36h. It compares received data with 3Eh. If the data does not match, then it sends ACK. If the data matches, it sends NACK and completes the communication by issuing Stop.

I2C Start	Slave Addr 36 + R	ACK	Read 3Eh? <b>'No'</b>	ACK	Read 3Eh? 'Yes'	NACK	I2C Stop
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### Method 2

In this method, the I<sup>2</sup>C sequence involves reading only one data byte for every sequence. The I<sup>2</sup>C master compares the received data with 3Eh. If the data matches, it stops polling for the 3Eh.

I2C Start	Slave Addr 36 + R	ACK	Read Data	NACK	I2C Stop
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#### 3. Master Erase

The Master Erase command erases all flash pages simultaneously. The steps to execute this command are shown below.

a. Send the I<sup>2</sup>C sequence for Master Erase. **Note:** This clears the password lock bit on successful Master Erase execution, which unlocks flash for flash programming commands (e.g., Load and Verify Code, Load, Verify, Dump).



- b. Wait 24ms (the typical time for Master Erase).
- c. Poll for 3Eh.
- d. Read the Get Status command and check the status byte for Master Erase Failed (i.e., status value 08).

# 4. Flash Programming

The UROM provides two commands to program data into the flash memory.

- Load Code (10h)
- Load and Verify Code (50h)

The Load Code command writes input data to the flash memory. The Load and Verify Code command writes input data to the flash memory and verifies the data by reading back from the flash memory after writing. This command takes a longer time to execute. However, the user

can save significant time by using the Load and Verify Code command in place of using the Load Code and Verify Code commands separately.

To program and verify the flash memory, the user can use one of the following methods.

- Load and Verify Code command (50h)
- Load Code command (10h) and Verify Code command (40h)
- Load Code command (10h) and Dump Code command (20h)

The UROM functions are executed with the following commands. These commands are used for flash programming in the three methods above.

- Load and Verify Code (50h)
- Load Code (10h)
- Verify Code (40h)
- Dump Code (20h)

Each command is explained below.

#### Load and Verify Code

This command writes data into the flash memory and verifies it by reading data from the flash memory.

The steps to implement this command are listed below.

a. Send the following I<sup>2</sup>C sequence for flash programming with the Load and Verify Code command.

I2C Start	Slave	e Addr 36h -	+ W	ACK	Cmd 50h	ACK	Length N	ACK	AddL	ACK	AddH	ACK
Byte 1	ACK	Byte 2	ACK			Byte n	ACK	I2C S	top			

- b. Poll for 3Eh.
- c. Read the Get Status command and check the status byte for Verify Failed (i.e., status value 05).

### Load Code

The Load Code command (10h) writes n number of bytes to the flash memory, starting from the input address. This command requires a number of bytes to write (in one bytes) and the starting address. The starting address is given in two bytes: AddH and AddL. The bootloader function calculates the address as (AddH \* 256 + AddL). The one byte data length limits the total number of bytes transferred in a single sequence to 255 bytes for this command. To verify the written data, the user can use the Verify Code command or the Dump Code command. The steps to implement the Load Code command are listed below.

- a. Use the Master Erase command or the Flash Page Erase command. Note: The Flash Page Erase command requires password unlock. See the Miscellaneous I<sup>2</sup>C Commands section for details.
- b. Send the following I<sup>2</sup>C sequence for flash programming with the Load Code command.

I2C	Start	Slave	e Addr 36h -	⊦ W	ACK	Cmd 10h	ACK	Length N	ACK	AddL	ACK	AddH	ACK
Byte	e 1	ACK	Byte 2	ACK			Byte n	ACK	I2C S	top			

- c. Poll for 3Eh.
- d. Read the Get Status command for any error.

#### Verify Code

The Verify Code command compares the data written to the flash with the given data. If the data does not match, it sets the Verify Failed bit in the status code byte [bit 5]. The steps to implement the Verify Code command are listed below.

- a. Unlock the password. (This is not required if the Master Erase command executed successfully.)
- b. Send the following I<sup>2</sup>C sequence for flash programming with the Verify Code command.

I2C Start	Slav	e Addr 36h -	+ W	ACK	Cmd 40h	ACK	Length N	ACK	AddL	ACK	AddH	ACK
Byte 1	ACK	Byte 2	ACK	<		Byte r	n ACK	I2C S	top			

- c. Poll for 3Eh.
- d. Read the Get Status command and check the status byte for Verify Failed (i.e., status value 05).

#### Dump Code

The Dump Code command reads the data from the flash memory and compares it to the data written. This command requires the starting address (sent in two bytes) and a number of bytes to read (in two bytes). The command sends out the flash data from the given address. The steps to implement the Dump Code command are listed below.

- a. Unlock the password. (This is not required if the Master Erase command executed successfully and the Load Code operation executed.)
- b. Send the following I<sup>2</sup>C sequence for the Dump Code with the starting address AddL:AddH and the number of bytes LengthL:LengthH (n = LengthH \* 256 + LengthL).

I2C Start	Slave Addr 3	6h + W	ACK	Cmd 20h	ACK							
02 ACł	K AddL	ACK	AddH	ACK	Length	nL .	ACK	LengthH	ACK			
l²C Restart	Slave Addr 36h + R	ACI	χ -	ead te1	ACK			Read Byte n	ACK	3Eh (n+1)	NACK	I2C Stop

- c. Send restart and read n bytes of data with ACK.
- d. Read 3Eh with NACK and issue Stop.

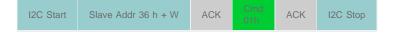
## 5. Get Status

The UROM provides the Get Status command, which returns flags and status code from the executed command. The I<sup>2</sup>C sequence for the Get Status command is shown below.

I2C Start	Slave Addr 36h + W	ACK	Cmd 04h	ACK						
estart	Slave Addr 36h + R	ACK	Read F	lags	ACK	Read Status Code	ACK	Read 3Eh	NACK	12C

## 6. Exit Bootloader

This command clears the I2C\_SPE bit, which is set by the Enter I<sup>2</sup>C Bootloader command, and generates an internal reset. **Note:** After receiving the Exit Bootloader command (01h), the I<sup>2</sup>C bootloader waits for approximately 32µs and then generates an internal reset.



# Miscellaneous I<sup>2</sup>C Commands

#### Password Unlock

The DS4830 has a 32-byte password in program memory at byte address 0020h through 003Fh. To access the password-protected commands, the user has to provide the same password using the Password Unlock command as shown below. Except for family 0 commands, all bootloader commands are password protected.

The sequence to unlock the password is as follows.

a. Send the following I<sup>2</sup>C sequence for Password Unlock.

I2C Start	Slave Addr 36h + W	ACK	Cmd 03h	ACK	PW0	ACK	PW1	ACK		ACK	PW31	ACK	I2C Stop	
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- b. Poll for 3Eh.
- c. Read the Get Status command and check bit 3 No Password Match of the status code byte.

Calculate CRC-16 of memory (code or data)

The UROM provides a function to calculate the CRC-16 of either program memory (code) or data memory (SRAM). The steps to calculate CRC-16 are as follows.

- a. Send the following I<sup>2</sup>C sequence to calculate the CRC-16. The CRC-16 values are two bytes prior to 3E.
- b. Wait for a delay of approximately (LengthL + LengthH \*256) \* 45µs.
- c. Send the following I<sup>2</sup>C sequence to read three bytes (two bytes CRC and the last byte 3E).

Note: The UROM takes approximately 45µs/byte to calculate the CRC-16.



#### Two-byte Read commands

The Read commands with two bytes of data (Table 2) use the following format to read bytes and complete the execution.

Table 2. I <sup>2</sup> C Bootloader Commands										
Command Name	Command	LSB	MSB							
Get Status	04h	Flags	Status							
Get Code Size (flash)	06h	Size-lower byte	Size-higher byte							
Get Data Size (SRAM)	07h	Size-lower byte	Size-higher byte							
Get Loader Version	08h	Lower version number	Higher version number							
Get Utility ROM Version	09h	Lower version number	Higher version number							

I2C Start Slave Addr 36h + W ACK Command ACK

I <sup>2</sup> C Restart Slave	Addr 36h + R ACK	Read LSB	ACK	Read MSB	ACK	Read 3Eh	NACK	I2C Stop
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### Get device specific banner (0Dh command)

The ID Banner command can be used to differentiate various MAXQ MCUs. The I<sup>2</sup>C sequence for the ID Banner command is shown below.

I2C Start	Slave Addr 36h + W	ACK	Cmd 0Dh	ACK						
I²C Restart	Slave Addr 36h + R	ACK	Read Byte1	ACK	 	Read Byte n	ACK	3E (n+1) Byte	NACK	I2C Stop

The n value for the DS4830 is 31 and the ID Banner is "DS4830 Loader 1.01 03-09-2010 \0" in ASCII.

### Code (Flash) Page Erase command

The DS4830 flash memory is divided into pages. Each page size is 512 bytes (256 words). In total, there are 128 pages in the flash memory. Each page can be erased individually using the I<sup>2</sup>C bootloader command. The steps to implement the Code (Flash) Page Erase command are shown below.

- a. Unlock the password (if locked).
- b. Send the following I<sup>2</sup>C sequence for the Flash Page Erase command.

I2C Start	Slave Addr 36h + W	ACK	Cmd E0h	ACK	00h	ACK	Page Num	ACK	00h	ACK	I2C Stop	
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- c. Wait 24ms (the typical time for Code (Flash) Page Erase).
- d. Poll for 3Eh.

# Additional Resources

Pseudocode for the I<sup>2</sup>C master (ZIP, 8kB)

# Notes

- 1. The I<sup>2</sup>C communication clock frequency should not be more than 100kHz for reliable operation.
- 2. Bootloader commands greater than 0Fh are password protected.

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