

General Description

- Latest Trench Power AlphaMOS (αMOS LV) technology
- Very Low $R_{DS(on)}$ at $4.5V_{GS}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

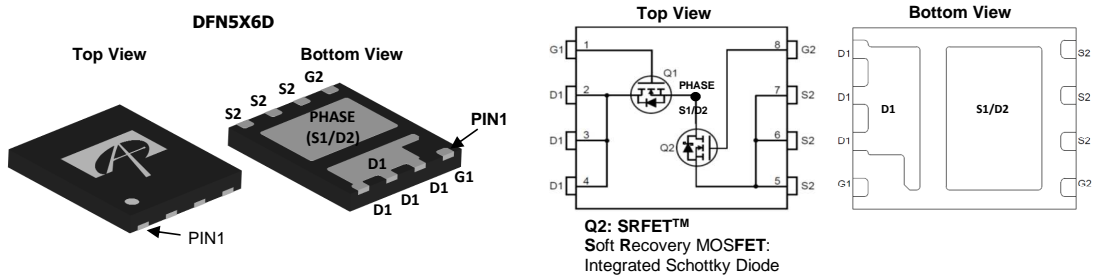
Application

- DC/DC Converters in Computing, Servers, and POL
- Isolated DC/DC Converters in Telecom and Industrial

Product Summary

	Q1	Q2
V_{DS}	30V	30V
I_D (at $V_{GS}=10V$)	58A	85A
$R_{DS(on)}$ (at $V_{GS}=10V$)	<5.4mΩ	<1.5mΩ
$R_{DS(on)}$ (at $V_{GS}=4.5V$)	<8.5mΩ	<2.3mΩ

100% UIS Tested
 100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units	
Drain-Source Voltage	V_{DS}	30		V	
Gate-Source Voltage	V_{GS}	±20	±20	V	
Continuous Drain Current	I_D	$T_C=25^\circ C$	58	85	A
		$T_C=100^\circ C$	36	66	
Pulsed Drain Current ^C	I_{DM}	135	340		
Continuous Drain Current	I_{DSM}	$T_A=25^\circ C$	24	42	A
		$T_A=70^\circ C$	19	33	
Avalanche Current ^C	I_{AS}	35	65	A	
Avalanche Energy $L=0.05mH$ ^C	E_{AS}	31	106	mJ	
V_{DS} Spike	V_{SPIKE}	36	36	V	
Power Dissipation ^B	P_D	$T_C=25^\circ C$	31	78	W
		$T_C=100^\circ C$	12	31	
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ C$	5	4.1	W
		$T_A=70^\circ C$	3.2	2.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C	

Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	20	25	25	30	°C/W
Maximum Junction-to-Ambient ^{A,D}		Steady-State	50	56	60	
Maximum Junction-to-Case	$R_{\theta JC}$	3.3	1.2	4	1.6	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.3	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		4.4	5.4	mΩ
		V _{GS} =4.5V, I _D =20A		6.7	8.5	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		80		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				35	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			1171		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		284		pF
C _{rss}	Reverse Transfer Capacitance			59		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.3	0.6	0.9	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		17	23	nC
Q _{g(4.5V)}	Total Gate Charge			8	11	nC
Q _{gs}	Gate Source Charge			4.7		nC
Q _{gd}	Gate Drain Charge			2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		6.5		ns
t _r	Turn-On Rise Time			15.5		ns
t _{D(off)}	Turn-Off DelayTime			17		ns
t _f	Turn-Off Fall Time			2.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		12.3		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		22.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

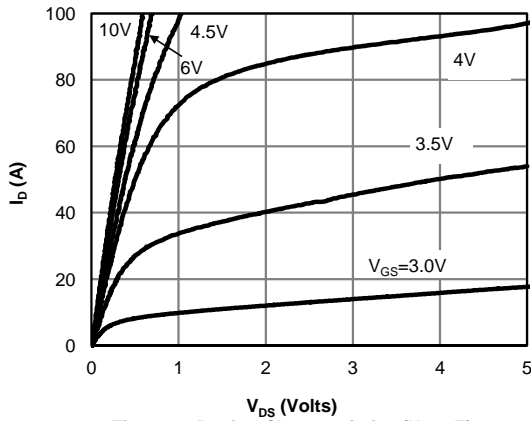


Figure 1: On-Region Characteristics (Note E)

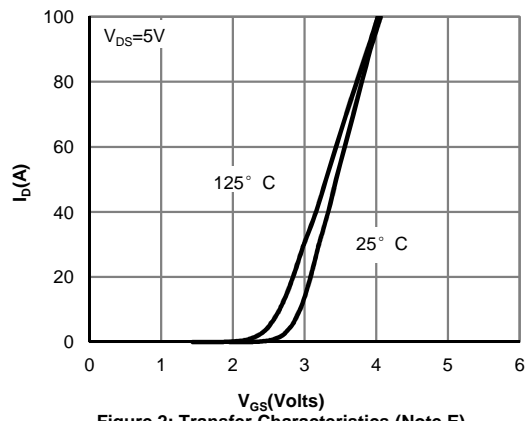


Figure 2: Transfer Characteristics (Note E)

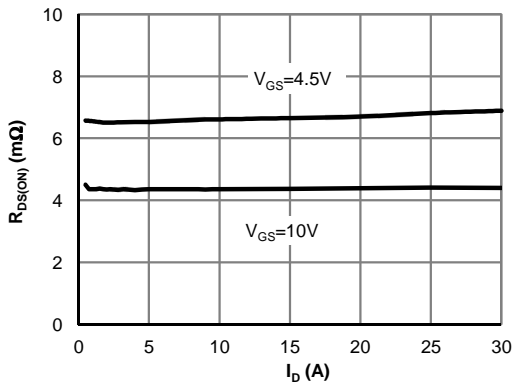


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

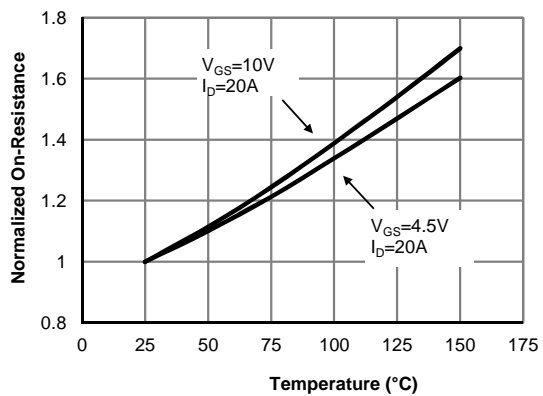


Figure 4: On-Resistance vs. Junction Temperature (Note E)

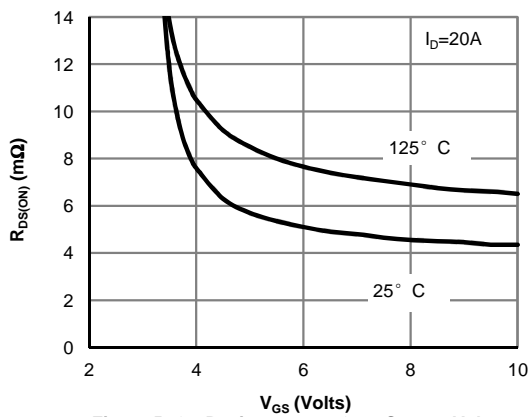


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

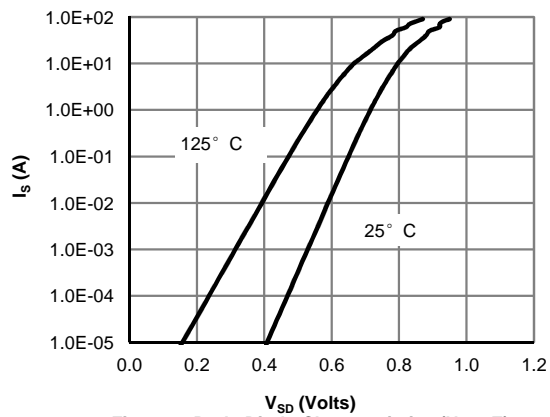


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

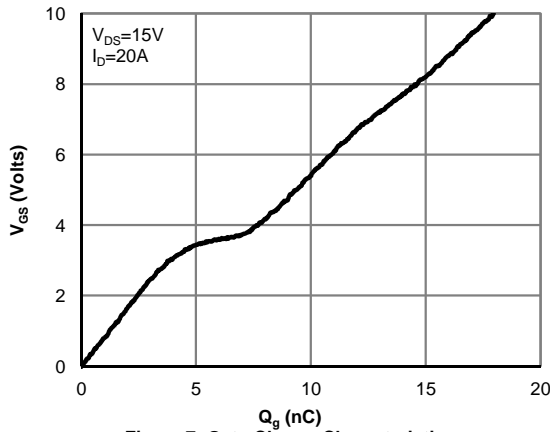


Figure 7: Gate-Charge Characteristics

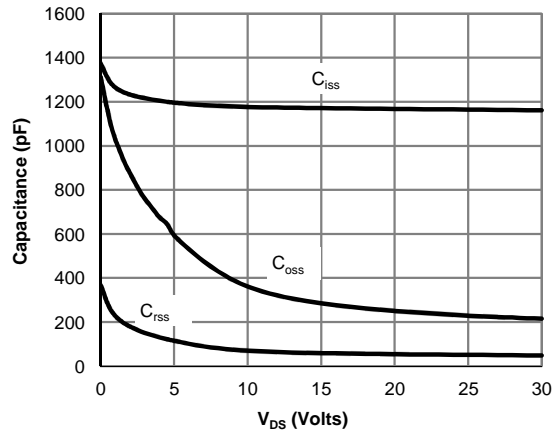


Figure 8: Capacitance Characteristics

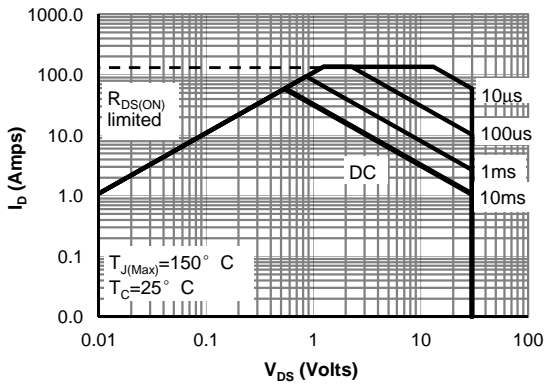


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

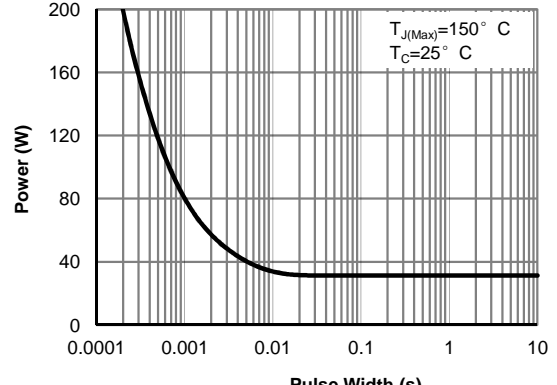


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

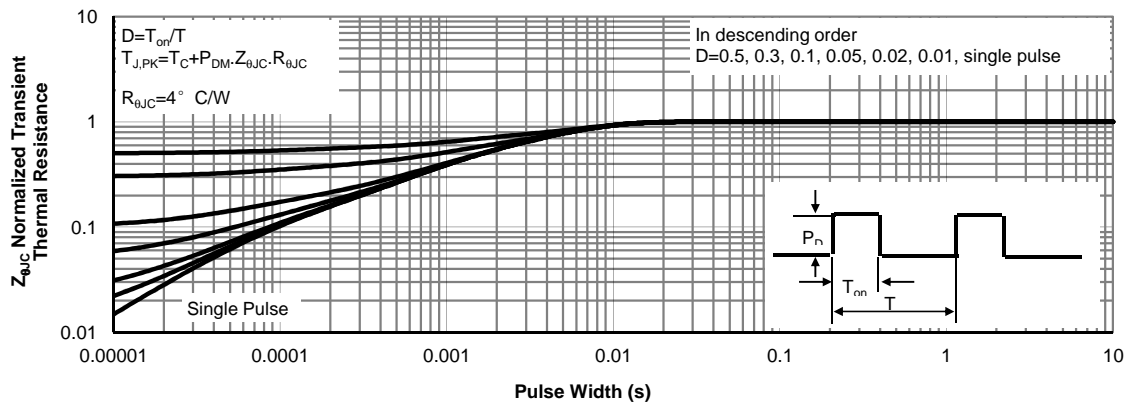


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

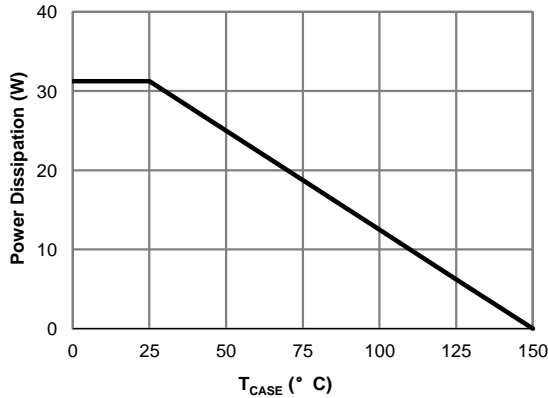


Figure 12: Power De-rating (Note F)

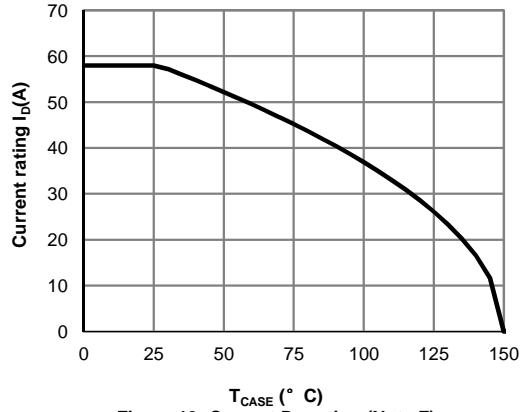


Figure 13: Current De-rating (Note F)

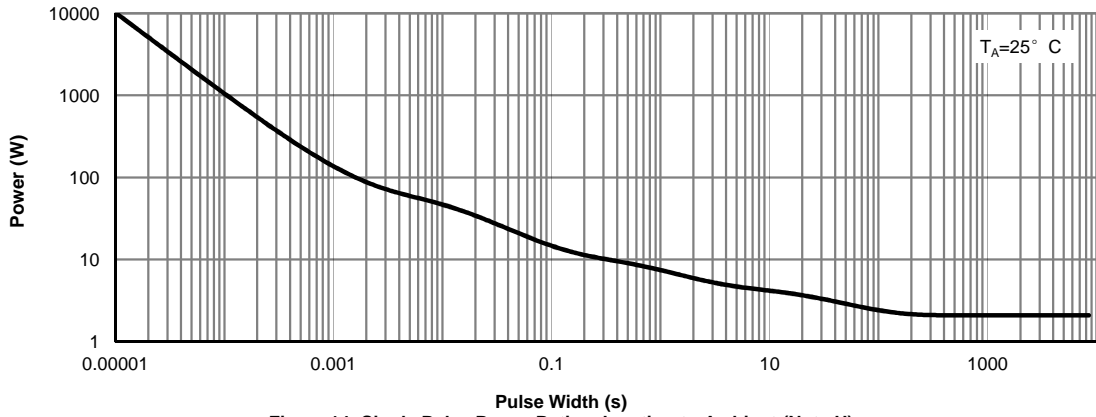


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

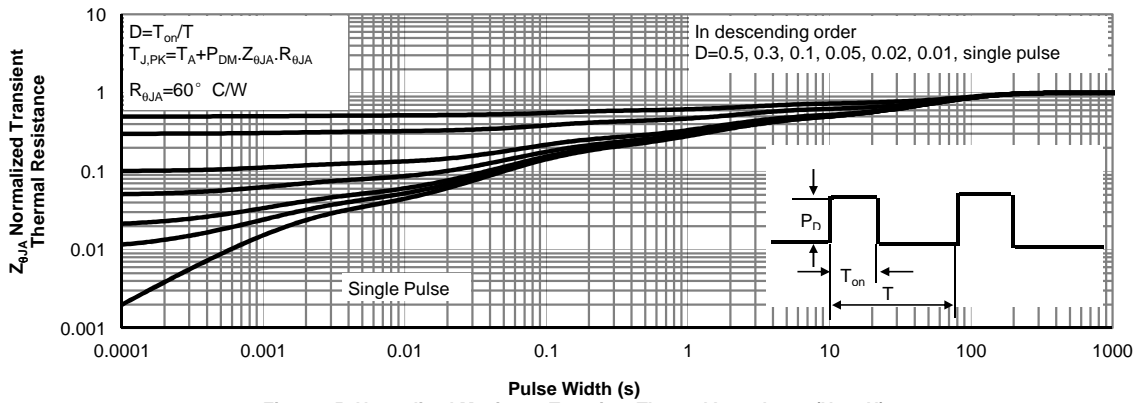


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			0.5 100	mA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.3	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		1.2	1.5	mΩ
		V _{GS} =4.5V, I _D =20A		1.6	2	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		100		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.46	0.6	V
I _S	Maximum Body-Diode Continuous Current ^G				85	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance			3973		pF
C _{oss}	Output Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz		1100		pF
C _{rss}	Reverse Transfer Capacitance			134		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.3	0.65	1	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =20A		60	85	nC
Q _{g(4.5V)}	Total Gate Charge			27	38	nC
Q _{gs}	Gate Source Charge			12		nC
Q _{gd}	Gate Drain Charge			10		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω		11.5		ns
t _r	Turn-On Rise Time			16		ns
t _{D(off)}	Turn-Off DelayTime			38		ns
t _f	Turn-Off Fall Time			7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs		20.8		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs		60		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J =25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

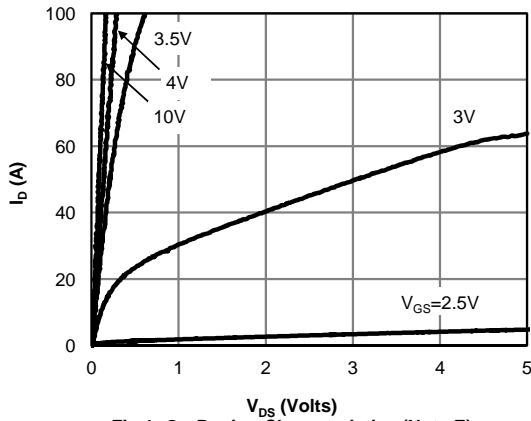


Fig 1: On-Region Characteristics (Note E)

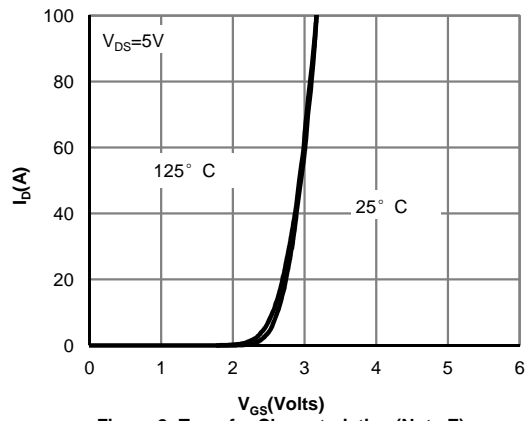


Figure 2: Transfer Characteristics (Note E)

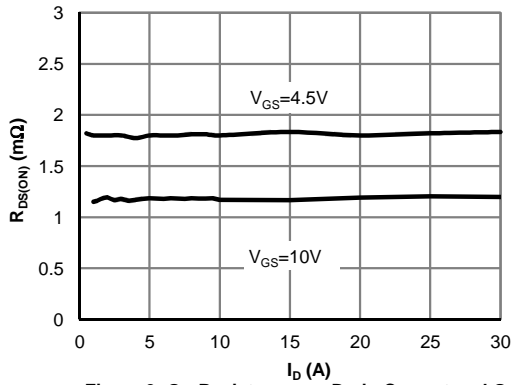


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

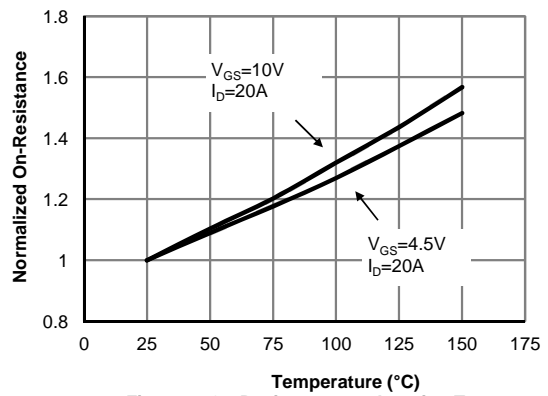


Figure 4: On-Resistance vs. Junction Temperature (Note E)

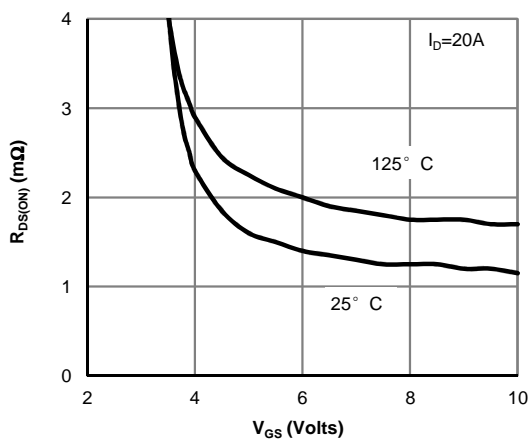


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

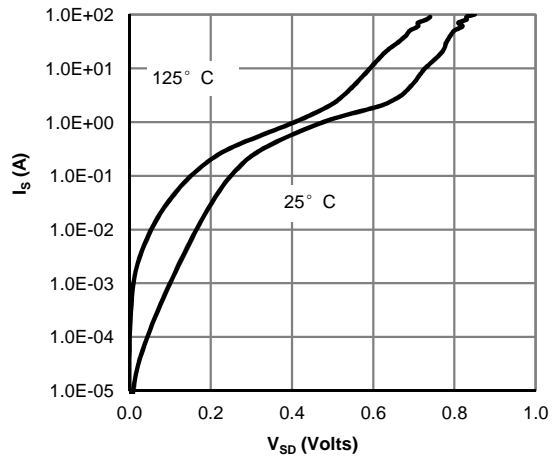


Figure 6: Body-Diode Characteristics (Note E)

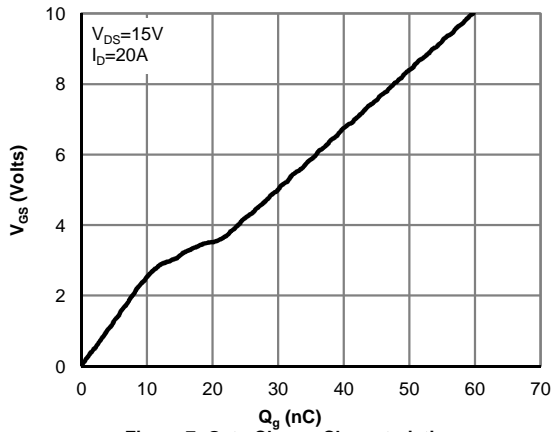


Figure 7: Gate-Charge Characteristics

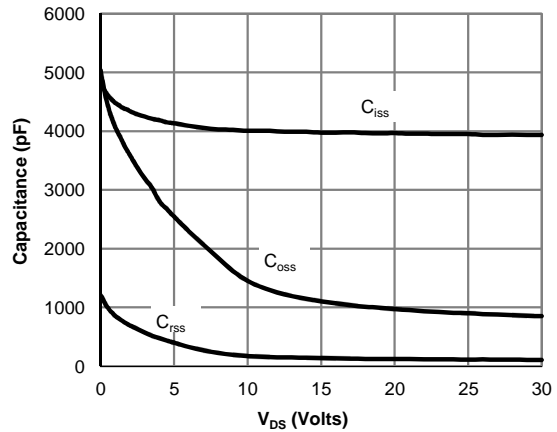


Figure 8: Capacitance Characteristics

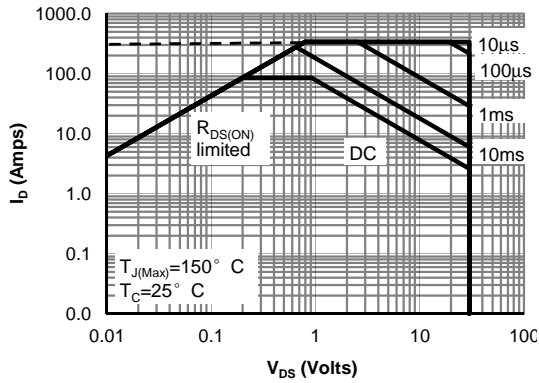


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

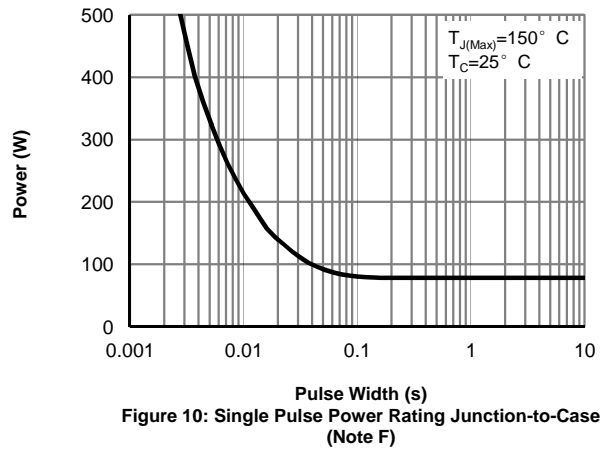


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

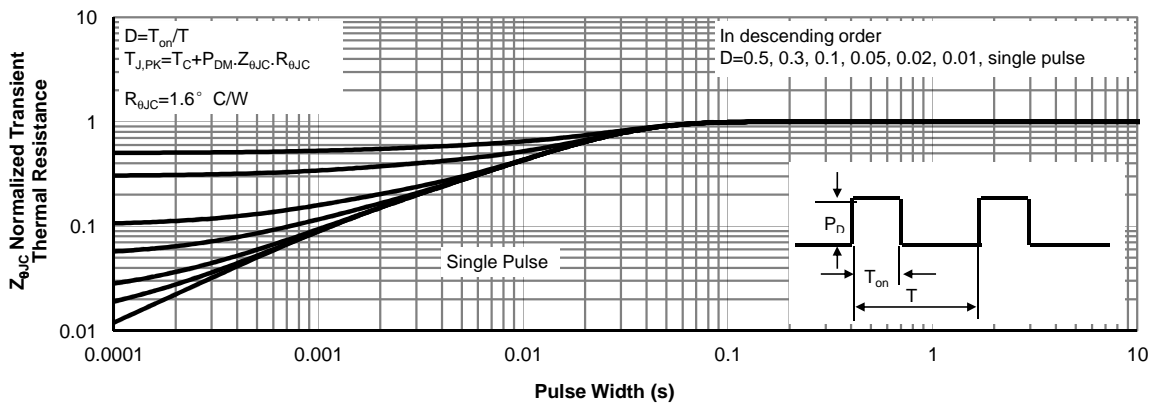


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

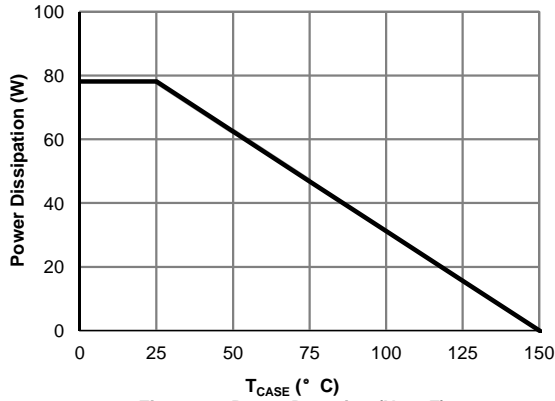


Figure 12: Power De-rating (Note F)

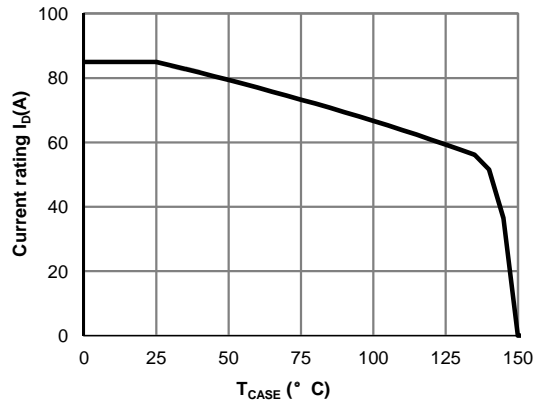


Figure 13: Current De-rating (Note F)



Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

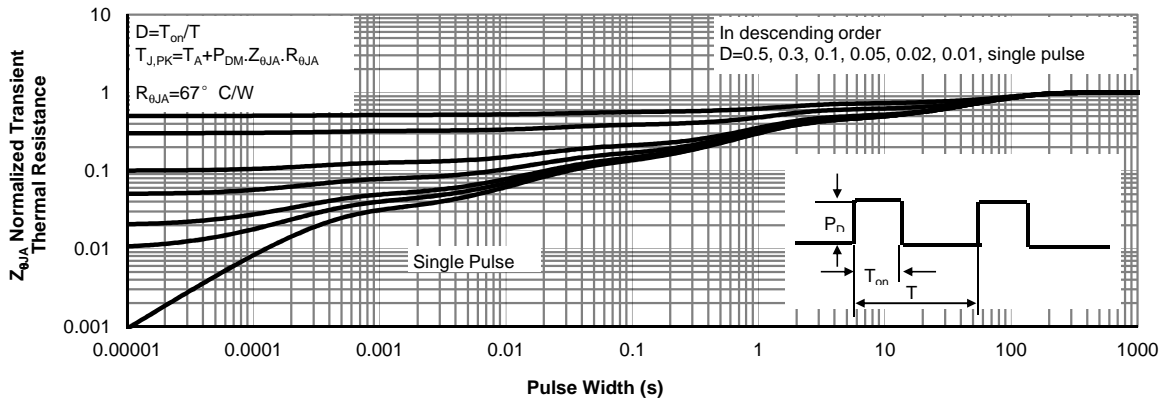
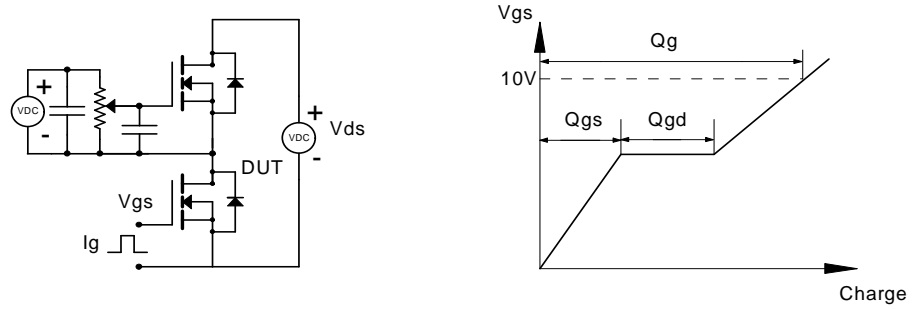
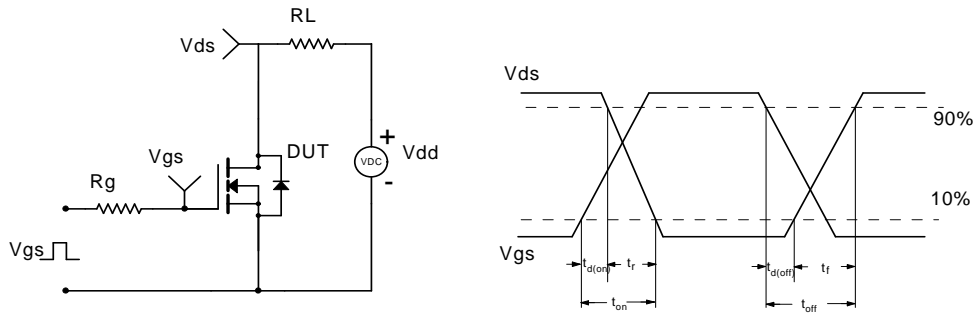


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

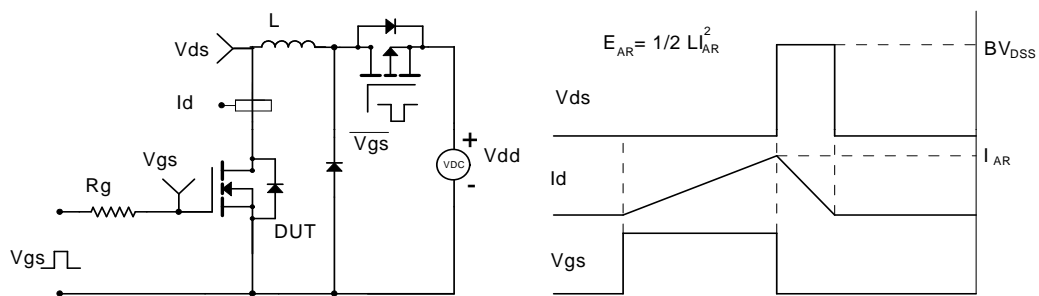
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

