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Vishay Siliconix

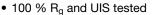
P-Channel 150 V (D-S) MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	-150			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0475			
Q _g typ. (nC)	31.8			
I _D (A)	-29			
Configuration	Single			

FEATURES

- TrenchFET® power MOSFET
- Very low R_{DS(ON)} minimizes power loss from conduction



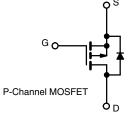
 Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Active clamp in DC/DC power supplies
- Battery protection
- · Load switch
- Motor drive control



ORDERING INFORMATION						
Package	PowerPAK SO-8					
Lead (Pb)-free and halogen-free	SiR873DP-T1-GE3					
ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	LIMIT	UNIT			
Drain-source voltage	V_{DS}	-150	V			
		00	v			

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	-150	V	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		-37		
	T _C = 70 °C	1	-29.6		
	T _A = 25 °C	l _D	_9 b, c		
	T _A = 70 °C		-7.2 ^{b, c}		
Pulsed drain current (t = 100 μs)		I _{DM}	50	Α	
Continuous source-drain diode current	T _C = 25 °C		37		
	T _A = 25 °C	I _S	5.6 ^{b, c}		
Single pulse avalanche current	. 0.1	I _{AS}	-40		
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	80	mJ	
Maximum power dissipation	T _C = 25 °C		104		
	T _C = 70 °C		66.6	W	
	T _A = 25 °C	P _D	6.25 ^{b, c}		
	T _A = 70 °C	1	4 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		
Soldering recommendations (peak temperature) c			260	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	15	20	°C/W		
Maximum junction-to-case (drain)	Steady state	R _{thJC}	0.9	1.2			

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 54 °C/W
- g. $T_C = 25$ °C



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-150	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = -250 μA	-	-92	-	m\//°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$			6.8	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-2	-	-4	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	-100	nA	
Zero gate voltage drain current		V _{DS} = -150 V, V _{GS} = 0 V	-	-	-1	μА	
	I _{DSS}	V _{DS} = -150 V, V _{GS} = 0 V, T _J = 70 °C	-	-	-15		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge -10 \text{ V}, V_{GS} = -10 \text{ V}$	-20	-	-	Α	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -10 A	-	0.0395	0.0475	Ω	
Forward transconductance ^a	9 _{fs}	V _{DS} = -15 V, I _D = -10 A	-	12	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	1805	-	pF	
Output capacitance	C _{oss}	$V_{DS} = -75 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	332	-		
Reverse transfer capacitance	C_{rss}		-	14.5	-		
Tatal asta shawa	0	V _{DS} = -75 V, V _{GS} = -10 V, I _D = -10 A	-	31.8	48		
Total gate charge	Q_g		-	25	-		
Gate-source charge	Q_{gs}	$V_{DS} = -75 \text{ V}, V_{GS} = -7.5 \text{ V}, I_{D} = -10 \text{ A}$	-	9.2	-	nC	
Gate-drain charge	Q _{gd}		-	9.5	-		
Output charge	Q _{oss}	$V_{DS} = -75 \text{ V}, V_{GS} = 0 \text{ V}$	-	68.8	-		
Gate resistance	R_g	f = 1 MHz	1.9	3.4	6	Ω	
Turn-on delay time	t _{d(on)}		-	15	30		
Rise time	t _r	V_{DD} = -75 V, R_L = 7.5 Ω , I_D \cong -10 A,	-	7	14	ns	
Turn-off delay time	t _{d(off)}	V_{GEN} = 10 V, R_g = 1 Ω	-	28	56		
Fall time	t _f		-	9	18		
Drain-Source Body Diode Characteristi	cs					•	
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	37	^	
Pulse diode forward current	I _{SM}		i	-	50	Α	
Body diode voltage	V_{SD}	I _S = -5 A, V _{GS} = 0 V	-	-0.79	-1.1	V	
Body diode reverse recovery time	t _{rr}		-	75	150	ns	
Body diode reverse recovery charge	Q _{rr}	100 A/ T 25 20	-	245	490	nC	
Reverse recovery fall time	ta	$I_F = -5 \text{ A, di/dt} = -100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$	-	58	-		
Reverse recovery rise time	t _b		_	17	-	ns	

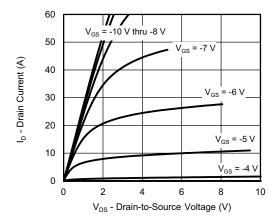
Notes

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

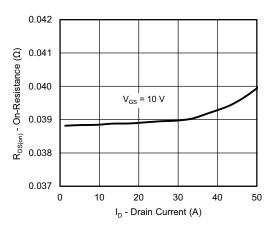
a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

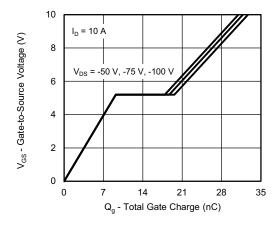




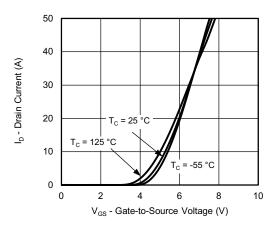
Output Characteristics



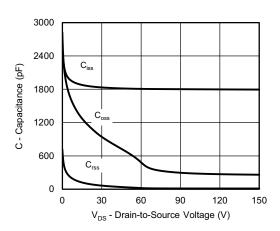
On-Resistance vs. Drain Current and Gate Voltage



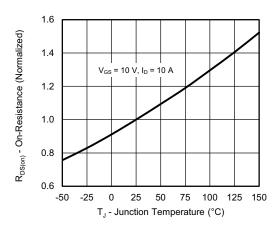
Gate Charge



Transfer Characteristics

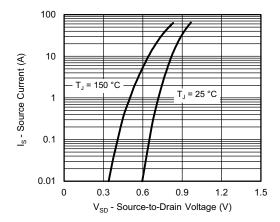


Capacitance

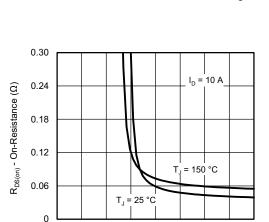


On-Resistance vs. Junction Temperature





Source-Drain Diode Forward Voltage

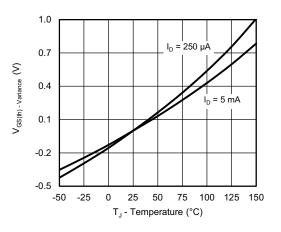


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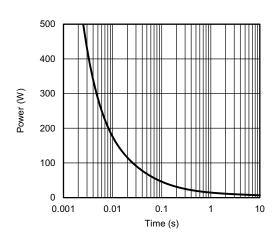
On-Resistance vs. Gate-to-Source Voltage

6

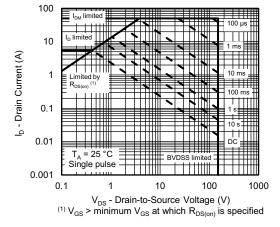
V_{GS} - Gate-to-Source Voltage (V)



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

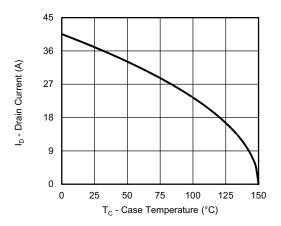


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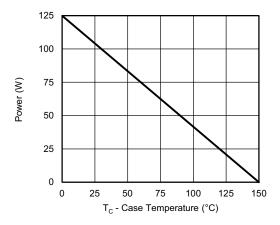
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Safe Operating Area, Junction-to-Ambient

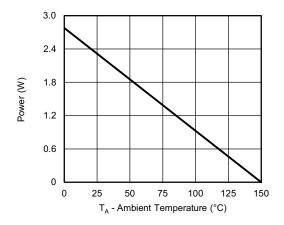




Current Derating a





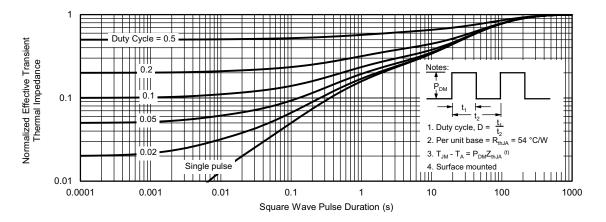


Power, Junction-to-Ambient

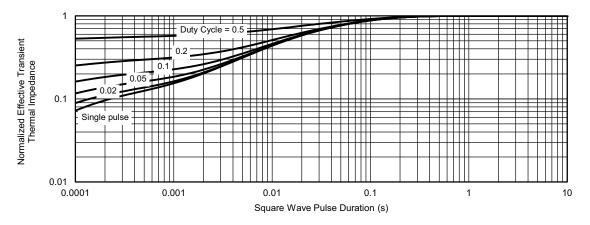
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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