Keywords: power dissipation, resistive loss, switching loss, power MOSFETs

TUTORIAL 1832

Power Supply Engineer's Guide to Calculate Dissipation for MOSFETs in High-Power Supplies

Dec 26, 2002

Abstract: Power MOSFETs are an integral part of any high-power-switching power supplies used in portable devices. Additionally, these MOSFETs are difficult components to specify for notebook products with minimal heat dissipation capabilities. This article provides step-by-step instructions for calculating the power dissipation of these MOSFETs and determining the temperature at which they operate. It then illustrates these concepts by stepping through the design of one 30A phase of a multiphase, synchronous-rectified, step-down CPU core supply.

Perhaps the toughest challenge that designers of portable power supplies face is powering modern high-performance CPUs. Recently, CPU supply currents have doubled every two years. In fact, today's portable core supplies can require up to 60A or more, at between 0.9V and 1.75V. But while current requirements have increased steadily, the space available for power supplies has not—a fact that has stretched thermal designs to the limit, and beyond.

Supplies with such high current are typically broken into two or more phases, with each phase handling between 15A and 30A. This approach eases component selection. A 60A supply, for example, essentially becomes two 30A supplies. But because this approach does not create additional board space, it hardly eases the thermal design challenge.

MOSFETs are the most difficult components to specify for high-current power supplies. This is especially true for notebook computers, an environment where heatsinks, fans, heatpipes, and other means of disposing heat are typically reserved for the CPU itself. Thus, the power supply often contends with cramped space, still air, and heat from nearby components. Moreover, nothing is available to aid power dissipation except a minimal amount of PC-board copper underneath the supply.

MOSFET selection begins by choosing devices that can handle the required current, given an adequate thermal dissipation path. Selection ends with quantifying the needed thermal dissipation and ensuring the dissipation path. This article provides step-by-step instructions for calculating the power dissipation of these MOSFETs and determining the temperature at which they operate. It then illustrates these concepts by stepping through the design of one 30A phase of a multiphase, synchronous-rectified, step-down CPU core supply.

Calculating MOSFET Power Dissipation

To determine whether or not a MOSFET is suitable for a particular application, you must calculate its power dissipation, which consists mainly of resistive and switching losses:

$$PD_{DEVICE\ TOTAL} = PD_{RESISTIVE} + PD_{SWITCHING}$$

Because a MOSFET's power dissipation depends greatly on its on-resistance, $R_{DS(ON)}$, calculating $R_{DS(ON)}$ seems a good place to start. But a MOSFET's $R_{DS(ON)}$ depends on its junction temperature, T_J. In turn, T_J depends on both the power dissipated in the MOSFET and the thermal resistance, Θ_{JA}, of the MOSFET. So, it is hard to know where to begin. As several terms within the power dissipation calculation are interdependent, an iterative process is useful to determine this number (**Figure 1**).
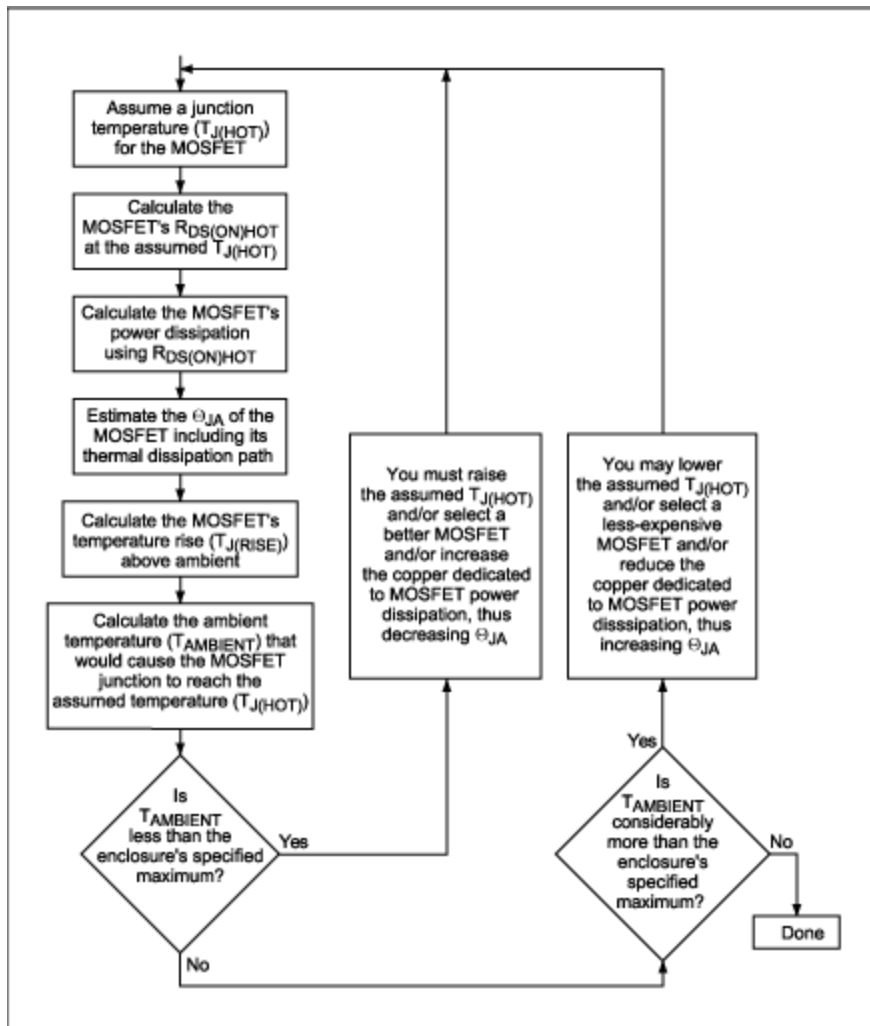

Figure 1. This flowchart represents the iterative process by which each of the MOSFETs (the synchronous rectifier and the switching MOSFET) is chosen. During this process, the junction temperature of each MOSFET is assumed, and both the MOSFETs' power dissipation and allowable ambient temperature are calculated. The process ends when the allowable ambient temperature is at, or slightly above the maximum temperature expected within the enclosure that houses the power supply and the circuitry which it powers.

The iterative process starts by first assuming a junction temperature for each MOSFET, then calculating each MOSFET's individual power dissipation and allowable ambient temperature. The process ends when the allowable ambient air temperature is at, or slightly above the expected maximum temperature within the enclosure that houses the power supply and other circuitry which it powers.

Making this calculated ambient temperature as high as possible may be tempting, but it is not usually a good idea. To do so would require a more expensive MOSFET, more copper underneath the MOSFET, or moving more air by a larger, faster fan—all of which is unwarranted.

In a sense, assuming a MOSFET junction temperature and then calculating an associated ambient temperature entails working backwards. After all, the ambient temperature determines the MOSFET's junction temperature—not the reverse. However, the calculations required when starting with an assumed junction temperature are easier to accomplish than when starting with an assumed ambient temperature and working from there.

For both the switching MOSFET and the synchronous rectifier, select a maximum permitted die junction temperature, $T_{J(HOT)}$, to use as a starting point for this iterative process. Most MOSFET data sheets only specify a maximum $R_{DS(ON)}$ at +25°C. But recently, some MOSFET documentation has listed maximums at +125°C as well. MOSFET $R_{DS(ON)}$ increases with temperature, exhibiting typical temperature coefficients that range from 0.35%/°C to 0.5%/°C (**Figure 2**).
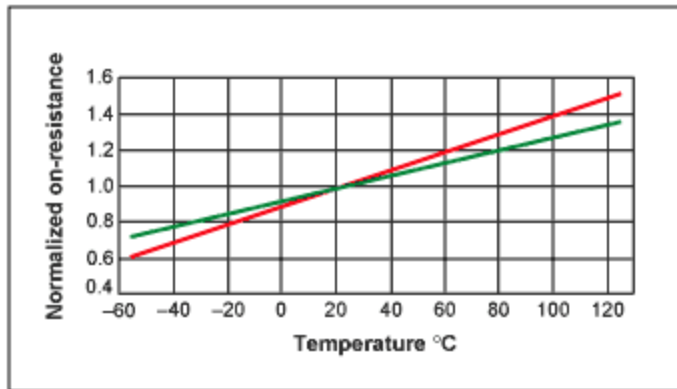

Figure 2. Typical power MOSFET on-resistance temperature coefficients range from 0.35% per degree (black line) to 0.5% per degree (red line).

If in doubt, use the more unfavorable temperature coefficient and the MOSFET's +25°C specification (or its +125°C specification, if available) to calculate an approximate maximum $R_{DS(ON)}$ at your chosen $T_{J(HOT)}$:

$$RDS_{(ON)HOT} = R_{DS(ON)SPEC} [1 + 0.005 \times (T_{J(HOT)} - T_{SPEC})]$$

where $R_{DS(ON)SPEC}$ is the MOSFET on-resistance used for the calculation, while T_{SPEC} is the temperature at which $R_{DS(ON)}SPEC$ is specified. Use the calculated $R_{DS(ON)}HOT$ to determine the power dissipation of both the synchronous rectifier and switching MOSFETs as described below.

The following paragraphs discuss calculating each MOSFET's power dissipation at its assumed die temperature, followed by the additional steps to complete this iterative process. (The entire procedure is detailed in Figure 1.)

The Synchronous Rectifier's Power Dissipation

For all but the lightest loads, the drain-to-source voltage of the synchronous rectifier's MOSFET is clamped by the catch diode during turn-on and turn-off. Therefore, the synchronous rectifier incurs no switching losses, making its power dissipation easy to calculate. Only resistive losses must be

considered.

The worst-case losses occur at the maximum duty factor of the synchronous rectifier, which occurs when the input voltage is at its maximum. Through the use of the synchronous rectifier's $R_{DS(ON)}$HOT and its duty factor, along with Ohm's Law, you can calculate its approximate power dissipation:

$$PD_{SYNCHRONOUS\ RECTIFIER} = [I_{LOAD}^2 \times R_{DS(ON)HOT}] \times [1 - (V_{OUT}/V_{INMAX})]$$

The Switching MOSFET's Power Dissipation

The switching MOSFET's resistive losses are calculated much as the synchronous rectifier's, using its (different) duty factor and $R_{DS(ON)HOT}$:

$$PD_{RESISTIVE} = [I_{LOAD}^2 \times R_{DS(ON)HOT}] \times (V_{OUT}/V_{IN})$$

Calculating the switching MOSFET's switching loss is difficult because it depends on many hard-to-quantify and typically unspecified factors that influence both turn-on and turn-off. Use the rough approximation in the following formula as the first step in evaluating a MOSFET and verify performance on the lab bench:

$$PD_{SWITCHING} = (C_{RSS} \times V_{IN}^2 \times f_{SW} \times I_{LOAD})/I_{GATE}$$

where C_{RSS} is the MOSFET's reverse-transfer capacitance (a data sheet parameter), f_{SW} is the switching frequency, and I_{GATE} is the MOSFET gate-driver's sink/source current at the MOSFET's turn-on threshold (the V_{GS} of the gate-charge curve's flat portion).

Once you have narrowed the choice to a specific generation of MOSFET based on cost (the cost of a MOSFET is very much a function of the specific generation to which it belongs), select the device within the generation that will minimize power dissipation. This is the device with equal resistive and switching losses. Using a smaller (faster) MOSFET increases resistive losses more than it decreases switching losses; a larger (low $R_{DS(ON)}$) device increases switching losses more than it decreases resistive losses.

If V_{IN} varies, calculate the switching MOSFET's power dissipation at both $V_{IN(MAX)}$ and $V_{IN(MIN)}$. The MOSFET's worst-case power dissipation will occur at either the minimum or the maximum input-voltage level. The dissipation is the sum of two functions: the resistive dissipation, which is highest at $V_{IN(MIN)}$ (the higher duty factor), and the switching dissipation, which is highest at $V_{IN(MAX)}$ (because of the V_{IN}^2 term). An optimal selection has roughly equal dissipations at the V_{IN} extremes, balancing resistive and switching dissipations across the V_{IN} range.

If the dissipation at $V_{IN(MIN)}$ is significantly higher, resistive losses dominate. In that case, consider a larger switching MOSFET (or more than one in parallel) to lower $R_{DS(ON)}$. But if the losses at $V_{IN(MAX)}$ are significantly higher, consider decreasing the size of the switching MOSFET (or removing a MOSFET if multiple devices are used) to allow it to switch faster.

If the resistive and switching losses balance, but are still too high, there are several ways to proceed:
- Change the problem definition. For example, redefine the input voltage range.
- Change the switching frequency to lower switching losses, possibly allowing a larger and lower $R_{DS(ON)}$ switching MOSFET.
- Increase the gate-driver current, possibly lowering switching losses. The MOSFET's own internal gate resistance, which ultimately limits the gate-driver current, places a practical limit on this approach.

- Use an improved MOSFET technology that might simultaneously switch faster, have lower $R_{DS(ON)}$, and have lower gate resistance.

Fine-tuning the MOSFET's size beyond a certain point may not be possible due to a limited choice of devices. Ultimately, it is the MOSFET's worst-case power that must be dissipated.

Thermal Resistance

The next step is the calculation of the ambient air temperature surrounding each MOSFET that would cause the assumed MOSFET junction temperature to be reached. (Refer to Figure 1 above for the iterative process to determine the right MOSFETs for both the synchronous rectifier and the switching MOSFET.) To make this calculation, first determine the junction-to-ambient thermal resistance, Θ_{JA}, of each MOSFET.

Thermal resistance can be difficult to estimate. While it is relatively easy to measure the Θ_{JA} of a single device on a simple PC board, it can be hard to predict thermal performance in an actual power supply within a system, where many heat sources compete for limited dissipation paths. If multiple MOSFETs are used in parallel, you can calculate their combined thermal resistance in the same way as the equivalent resistance of two or more paralleled resistors.

Start with the MOSFET's Θ_{JA} specification. For single-die, 8-pin SO MOSFET packages, Θ_{JA} is usually near 62°C/W. For other packages with thermal tabs or exposed heat slugs, it may range between 40°C/W to 50°C/W (**Table 1**).

Table 1. Typical Thermal Resistances of MOSFET Packages

Package	θ_{JA} (°C/W) Minimum Footprint	θ_{JA} (°C/W) 1in2 of 2oz Copper	θ_{JA} (°C/W)
SOT-23 (thermally enhanced)	270	200	75
SOT-89	160	70	35
SOT-23	110	45	15
µMAX-8/Micro8 (thermally enhanced)	160	70	35
TSSOP-8	200	100	45
SO-8 (thermally enhanced)	125	62.5	25
D-PAK	110	50	3
D2-PAK	70	40	2

Note: Thermal resistances vary among individual devices in the same package type and among similar packages from different manufacturers, depending on package mechanical characteristics, die size, and mounting and bonding method. Carefully consider thermal information in the MOSFET data sheet.

To calculate the MOSFET's die temperature rise above ambient, use the following equation:

$T_{J(RISE)} = PD_{DEVICE\ TOTAL} \times \Theta_{JA}$

Next, calculate the ambient temperature that will cause the die to reach the assumed $T_{J(HOT)}$:

$T_{AMBIENT} = T_{J(HOT)} - T_{J(RISE)}$

If the calculated $T_{AMBIENT}$ is lower than the enclosure's maximum specified ambient temperature (meaning that the enclosure's maximum specified ambient temperature will cause the MOSFET's assumed $T_{J(HOT)}$ to be exceeded), you must do one or more of the following:

- Raise the assumed $T_{J(HOT)}$, but not above the data sheet maximum.
- Lower the MOSFET power dissipation by choosing a more suitable MOSFET.
- Decrease Θ_{JA} by increasing the airflow or the amount of copper around the MOSFET.

Recalculate $T_{AMBIENT}$. (Employing a spreadsheet simplifies the multiple iterations typically required to select an acceptable design.)

Alternatively, if the calculated $T_{AMBIENT}$ is higher than the enclosure's maximum specified ambient temperature by a fair amount, any or all of the following optional steps can be taken:

- Lower the assumed $T_{J(HOT)}$.
- Reduce the copper dedicated to the MOSFET's power dissipation.
- Use a less expensive MOSFET.

These last steps are optional as, in this case, the MOSFET will not be damaged by excessive temperature. However, these steps reduce both board area and cost as long as the calculated $T_{AMBIENT}$ remains higher than the enclosure's maximum temperature by some margin.

The biggest source of inaccuracy in this procedure is Θ_{JA}. Carefully read any data sheet notes associated with a Θ_{JA} specification. Typical specifications assume a device mounted on 1in² of 2oz copper. The copper performs much of the power dissipation, and different amounts of copper change Θ_{JA} dramatically. For example, the Θ_{JA} of a D-Pak might be 50°C/W with 1in² of copper. But with copper underlying just the package footprint, the Θ_{JA} more than doubles (Table 1).

With multiple MOSFETs in parallel, the Θ_{JA} depends mostly on the copper area to which they are mounted. The equivalent Θ_{JA} for two devices can be half that of one device, but only if the copper area is also doubled. That is, adding a parallel MOSFET without additional copper halves the $R_{DS(ON)}$, but changes Θ_{JA} much less.

Lastly, Θ_{JA} specifications assume that no other devices contribute heat to the copper dissipation area. At high currents, every component in the power path, even PC-board copper, generates heat. To avoid overheating the MOSFETs, carefully estimate the q_{JA} that the physical situation can realistically achieve and consider the following:

- Study the selected MOSFET's available thermal information.
- Investigate whether or not there is space available for additional copper, heatsinks, and other devices.
- Determine if increasing airflow is feasible.
- See if other devices contribute significant heat to the assumed dissipation path.
- Estimate excess heating or cooling from nearby components and spaces.

Design Example

The CPU core supply shown in **Figure 3** delivers 1.5V at 60A. Two identical 30A power stages operating at 300kHz supply the 60A output current. The MAX1544 IC drives two stages in a single solution, using two phases that are 180° out-of-phase.The supply's input range spans from 7V to 24V, with the specified maximum ambient temperature of the enclosure at +60°C.
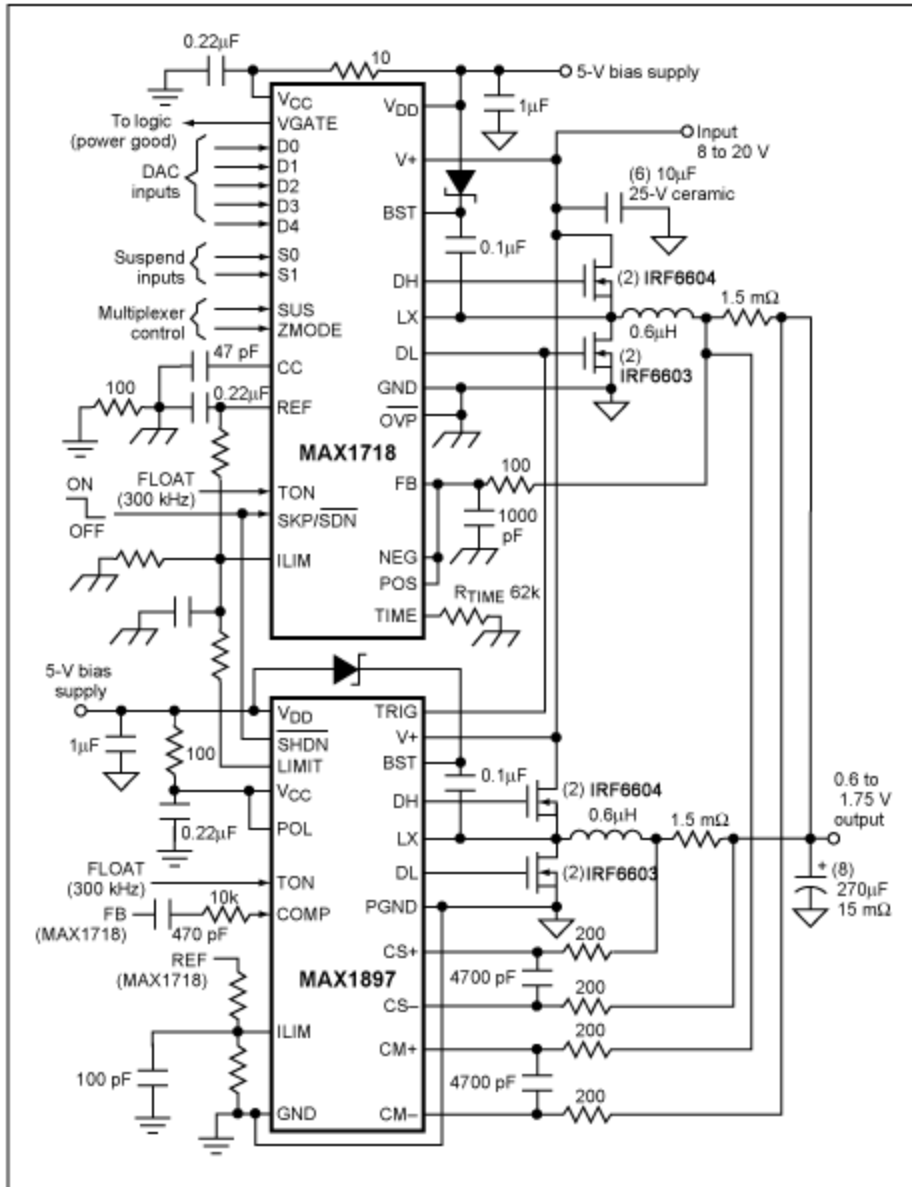
Figure 3. The MOSFETs for this step-down switching regulator were chosen using the iterative process described in this article. Board designers commonly use this type of switching regulator to power modern high-performance CPUs.

The synchronous rectifier comprises two IRF6603 MOSFETs in parallel, with a combined maximum $R_{DS(ON)}$ of 2.75mΩ at room temperature and approximately 4.13mΩ at +125°C (the assumed $T_{J(HOT)}$). With a maximum duty factor of 94%, a 30A load current, and a 4.13mΩ maximum $R_{DS(ON)}$, these paralleled MOSFETs dissipate about 3.5W. Supplied with 2in² of copper to dissipate that power, the overall Θ_{JA} should be about 18°C/W. Note that this thermal resistance value is taken from the MOSFET data sheet. The temperature rise of the combined MOSFETs will be approximately +63°C, so this design will work with an ambient temperature up to +60°C.

The switching MOSFET has two IRF6604 MOSFETs in parallel, with a combined maximum $R_{DS(ON)}$ of 6.5mΩ at room temperature and approximately 9.75mΩ at +125°C (the assumed $T_{J(HOT)}$). The combined

C_{RSS} is 380pF. The MAX1544 high-side, 1Ω gate drivers deliver approximately 1.6A. At V_{IN} = 7V, the resistive losses are 1.63W and the switching losses are approximately 0.105W. At V_{IN} = 24V, the resistive losses are 0.475W and the switching losses are approximately 1.23W. Total losses at each input operating point are approximately equal and the worst-case total loss is 1.74W at the minimum V_{IN}.

With a Θ_{JA} of about 28°C/W, the expected temperature rise is +46°C, which enables operation up to an ambient temperature of about +80°C. With an ambient temperature higher than the enclosure's maximum specified temperature, the designer may choose to reduce the copper area dedicated for the MOSFET, though this step is optional. The copper areas in this example are required for the MOSFETs alone. If other devices dissipate heat into those areas, more copper area will likely be required. If space is not available for the additional copper, reduce the total power dissipation, spread the heat to areas of low dissipation, or use active means to remove heat.

Conclusion

Thermal management is one of the most difficult facets/challenges of high-power portable design. This difficulty makes the iterative process outlined above necessary. Although this process should bring the board designer close to the final design, lab work must ultimately determine whether the design process was sufficiently accurate. Calculating the MOSFETs' thermal properties and ensuring their dissipation paths, while checking those calculations in the lab, help guarantee a robust thermal design.

Reprinted with permission from *Electronic Design*, October 14, 2002. Copyright 2002, Penton Media, Inc.

Related Parts		
MAX1718	Notebook CPU Step-Down Controller for Intel Mobile Voltage Positioning (IMVP-II)	Free Samples
MAX1897	Quick-PWM Slave Controllers for Multiphase, Step-Down Supplies	

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 1832: http://www.maximintegrated.com/an1832
TUTORIAL 1832, AN1832, AN 1832, APP1832, Appnote1832, Appnote 1832
© 2012 Maxim Integrated Products, Inc.
Additional Legal Notices: http://www.maximintegrated.com/legal