SBS 1.1-Compliant Gas Gauge and Protection Enabled With Impedance Track™ and External Battery Heater Control

Check for Samples: bq34z651

FEATURES

- **Next Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries**
  - **Better Than 1% Error Over the Lifetime of the Battery**
- **Supports the Smart Battery Specification SBS v1.1**
- **Flexible Configuration for 2-Series to 4-Series Li-Ion and Li-Polymer Cells**
- **Battery Temperature Heater Control**
- **Powerful 8-Bit RISC CPU with Ultralow Power Modes**
- **Full Array of Programmable Protection Features**
  - **Voltage, Current, and Temperature**
- **Satisfies JEITA Guidelines**
- **Added Flexibility to Handle More Complex Charging Profiles**
- **Lifetime Data Logging**
- **Drives 3-, 4-, and 5-Segment LED Display for Battery-Pack Conditions**
- **Supports SHA-1 Authentication**
- **Complete Battery Protection and Gas Gauge Solution in One Package**
- **Available in a 44-Pin TSSOP (DBT) package**

APPLICATIONS

- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq34z651 SBS-compliant gas gauge and protection IC, incorporating patented Impedance Track™ technology, is a single IC solution designed for battery-pack or in-system installation. The bq34z651 measures and maintains an accurate record of available charge in Li-Ion or Li-Polymer batteries using its integrated high-performance analog peripherals. The bq34z651 monitors capacity change, battery impedance, open-circuit voltage, and other critical parameters of the battery pack, which reports the information to the system host controller over a serial-communication bus. Together with the integrated analog front-end (AFE) short-circuit and overload protection, the bq34z651 maximizes functionality and safety while minimizing external component count, cost, and size in smart battery circuits.

The implemented Impedance Track gas gauging technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables remaining capacity to be calculated with discharge rate, temperature, and cell aging—all accounted for during each stage of every cycle with high accuracy.

Table 1. AVAILABLE OPTIONS

T_A	PACKAGE(1)	
	44-PIN TSSOP (DBT) Tube	44-PIN TSSOP (DBT) Tape and Reel
–40°C to 85°C	bq34z651DBT(2)	bq34z651DBTR(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) A single tube quantity is 40 units.
(3) A single reel quantity is 2000 units.

THERMAL INFORMATION

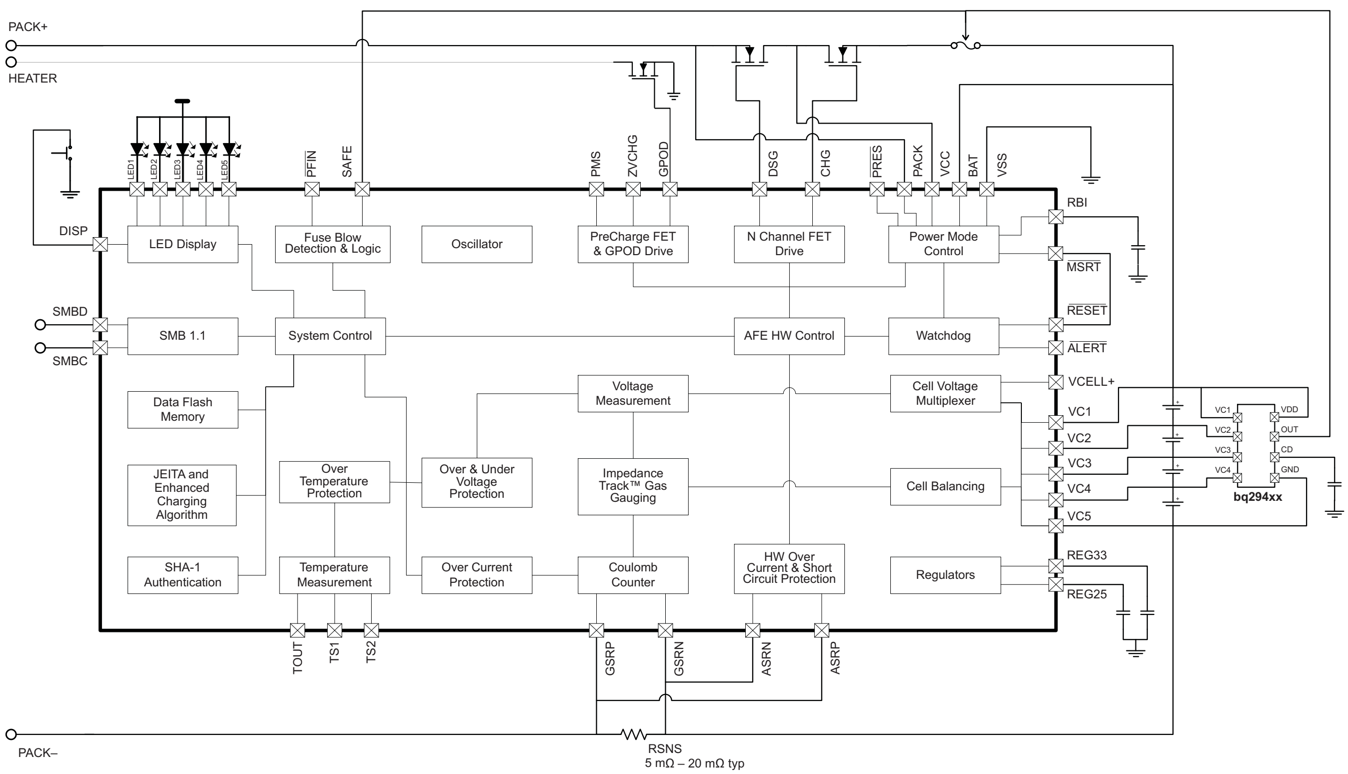
THERMAL METRIC[1]		bq34z651 TSSOP 44 PINS	UNITS
$\theta_{JA,\ High\ K}$	Junction-to-ambient thermal resistance[2]	60.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance [3]	15.3	
θ_{JB}	Junction-to-board thermal resistance [4]	30.2	
ψ_{JT}	Junction-to-top characterization parameter [5]	0.3	
ψ_{JB}	Junction-to-board characterization parameter [6]	27.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance [7]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

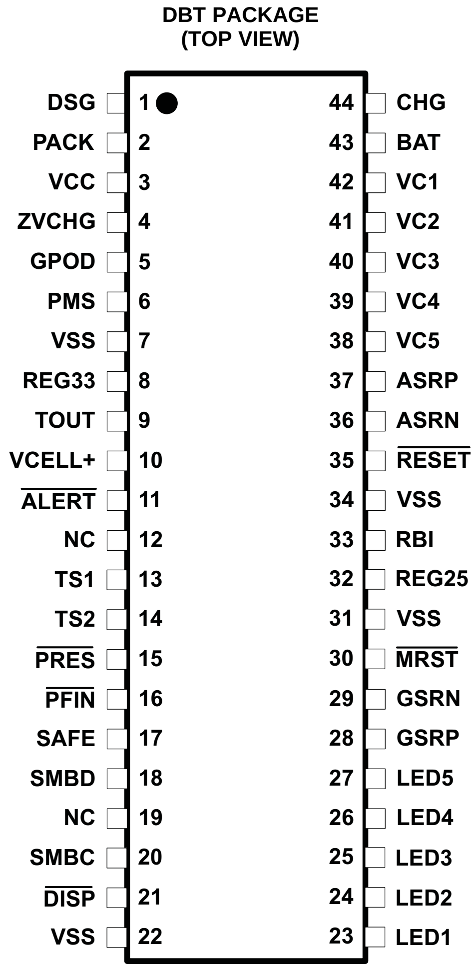
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SYSTEM PARTITIONING DIAGRAM



PACKAGE PINOUT DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O(1)	DESCRIPTION
NO.	NAME		
1	DSG	O	High-side N-channel discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wake up when device is in shutdown mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input.
4	ZVCHG	O	P-channel pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. It can be configured to be used in pre-charge condition.
6	PMS	I	Pre-charge mode setting input. Connect to PACK to enable 0v pre-charge using charge FET connected at CHG pin. Connect to VSS to disable 0-V pre-charge using charge FET connected at CHG pin.
7	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
8	REG33	P	3.3-V regulator output. Connect at least a 2.2-μF capacitor to REG33 and VSS.
9	TOUT	P	Thermistor bias supply output
10	VCELL+	—	Internal cell voltage multiplexer and amplifier output. Connect a 0.1-μF capacitor to VCELL+ and VSS.
11	$\overline{\text{ALERT}}$	I/OD	Alert output. In case of short circuit condition, overload condition and watchdog timeout, this pin will be triggered.
12	NC	—	Not used—leave floating.
13	TS1	IA	1st thermistor voltage input connection to monitor temperature
14	TS2	IA	2nd thermistor voltage input connection to monitor temperature
15	$\overline{\text{PRES}}$	I	Active low input to sense system insertion. Typically requires additional ESD protection.
16	$\overline{\text{PFIN}}$	I	Active low input to detect secondary protector status, and to allow the bq34z651 to report the status of the 2nd-level protection input
17	SAFE	O	Active high output to enforce additional level of safety protection; e.g., fuse blow
18	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq34z651
19	NC	—	Not used—leave floating.
20	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq34z651
21	$\overline{\text{DISP}}$	I/OD	Display control for the LEDs. This pin is typically connected to VCC via a 100-kΩ resistor and a push button switch connected to VSS.
22	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
23	LED1	I	LED1 display segment that drives an external LED depending on the firmware configuration
24	LED2	I	LED2 display segment that drives an external LED depending on the firmware configuration
25	LED3	I	LED3 display segment that drives an external LED depending on the firmware configuration
26	LED4	I	LED4 display segment that drives an external LED depending on the firmware configuration
27	LED5	I	LED5 display segment that drives an external LED depending on the firmware configuration
28	GSRP	IA	Coulomb counter differential input. Connect to one side of the sense resistor.
29	GSRN	IA	Coulomb counter differential input. Connect to one side of the sense resistor.
30	$\overline{\text{MRST}}$	I	Master reset input that forces the device into reset when held low. Must be held high for normal operation. Connect to $\overline{\text{RESET}}$ for correct operation of device.
31	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
32	REG25	P	2.5-V regulator output. Connect at least a 1-mF capacitor to REG25 and VSS.
33	RBI	P	RAM/Register backup input. Connect a capacitor to this pin and VSS to protect loss of RAM/Register data in case of short circuit condition.
34	VSS	P	Negative supply voltage input. Connect all VSS pins together for operation of device.
35	$\overline{\text{RESET}}$	O	Reset output. Connect to $\overline{\text{MSRT}}$.
36	ASRN	IA	Short circuit and overload detection differential input. Connect to sense resistor.
37	ASRP	IA	Short circuit and overload detection differential input. Connect to sense resistor.

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

TERMINAL FUNCTIONS (continued)

TERMINAL NO.	TERMINAL NAME	I/O (1)	DESCRIPTION
38	VC5	IA, P	Cell voltage sense input and cell balancing input for the negative voltage of the bottom cell in cell stack.
39	VC4	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the bottom cell and the negative voltage of the second lowest cell in cell stack.
40	VC3	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second lowest cell in cell stack and the negative voltage of the second highest cell in 4-series cell applications.
41	VC2	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the second highest cell and the negative voltage of the highest cell in 4-series cell applications. Connect to VC3 in 2-series cell stack applications.
42	VC1	IA, P	Cell voltage sense input and cell balancing input for the positive voltage of the highest cell in cell stack in 4-series cell applications. Connect to VC2 in 3-series or 2-series cell stack applications.
43	BAT	I, P	Battery stack voltage sense input
44	CHG	O	High-side N-channel charge FET gate drive

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature (unless otherwise noted) (1)

		PIN	UNIT
V_{SS}	Supply voltage range	BAT, VCC	–0.3 V to 34 V
		PACK, PMS	–0.3 V to 34 V
		VC(n) – VC(n+1); n = 1, 2, 3, 4	–0.3 V to 8.5 V
		VC1, VC2, VC3, VC4	–0.3 V to 34 V
		VC5	–0.3 V to 1 V
V_{IN}	Input voltage range	$\overline{\text{PFIN}}$, $\overline{\text{SMBD}}$, SMBC. LED1, LED2, LED3, LED4, LED5, $\overline{\text{DISP}}$	–0.3 V to 6 V
		TS1, TS2, SAFE, VCELL+, $\overline{\text{PRES}}$, $\overline{\text{ALERT}}$	–0.3 V to $V_{(REG25)}$ + 0.3 V
		$\overline{\text{MRST}}$, GSRN, GSRP, RBI	–0.3 V to $V_{(REG25)}$ + 0.3 V
		ASRN, ASRP	–1 V to 1 V
V_{OUT}	Output voltage range	DSG, CHG, GPOD	–0.3 V to 34 V
		ZVCHG	–0.3 V to $V_{(BAT)}$
		TOUT, $\overline{\text{ALERT}}$, REG33	–0.3 V to 6 V
		$\overline{\text{RESET}}$	–0.3 V to 7 V
		REG25	–0.3 V to 2.75 V
I_{SS}	Maximum combined sink current for input pins	$\overline{\text{PRES}}$, $\overline{\text{PFIN}}$, SMBD, SMBC, LED1, LED2, LED3, LED4, LED5	50 mA
T_A	Operating free-air temperature range		–40°C to 85°C
T_F	Functional temperature		–40°C to 100°C
T_{stg}	Storage temperature range		–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage	VCC, BAT	4.5		25	V
$V_{(STARTUP)}$	Minimum startup voltage	VCC, BAT, PACK	5.5			V

RECOMMENDED OPERATING CONDITIONS (continued)

Over operating free-air temperature range (unless otherwise noted)

		PIN	MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage Range	VC(n) – VC(n+1); n = 1,2,3,4	0		5	V
		VC1, VC2, VC3, VC4	0		V_{SUP}	V
		VC5	0		0.5	V
		ASRN, ASRP	–0.5		0.5	V
		PACK, PMS	0		25	V
$V_{(GPOD)}$	Output Voltage Range	GPOD	0		25	V
$A_{(GPOD)}$	Drain Current(1)	GPOD			1	mA
$C_{(REG25)}$	2.5-V LDO Capacitor	REG25	1			μF
$C_{(REG33)}$	3.3-V LDO Capacitor	REG33	2.2			μF
$C_{(VCELL+)}$	Cell Voltage Output Capacitor	VCELL+	0.1			μF
$C_{(PACK)}$	PACK input block resistor(2)	PACK	1			kΩ

(1) Use an external resistor to limit the current to GPOD to 1 mA in high voltage application.
(2) Use an external resistor to limit the in-rush current PACK pin required.

ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 μF, $C_{(REG33)}$ = 2.2 μF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{(NORMAL)}$	Firmware running			550		μA
$I_{(SLEEP)}$	Sleep Mode	CHG FET on; DSG FET on		124		μA
		CHG FET off; DSG FET on		90		μA
		CHG FET off; DSG FET off		52		μA
$I_{(SHUTDOWN)}$	Shutdown Mode			0.1	1	μA
SHUTDOWN WAKE; T_A = 25°C (unless otherwise noted)						
$I_{(PACK)}$	Shutdown exit at $V_{STARTUP}$ threshold				1	μA
SRx WAKE FROM SLEEP; T_A = 25°C (unless otherwise noted)						
$V_{(WAKE)}$	Positive or negative wake threshold with 1.00 mV, 2.25 mV, 4.5 mV and 9 mV programmable options		1.25		10	mV
$V_{(WAKE\_ACR)}$	Accuracy of $V_{(WAKE)}$	$V_{(WAKE)}$ = 1 mV; $I_{(WAKE)}$= 0, RSNS1 = 0, RSNS0 = 1;	–0.7		0.7	mV
		$V_{(WAKE)}$ = 2.25 mV; $I_{(WAKE)}$ = 1, RSNS1 = 0, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0;	–0.8		0.8	
		$V_{(WAKE)}$ = 4.5 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1; $I_{(WAKE)}$ = 0, RSNS1 = 1, RSNS0 = 0;	–1.0		1.0	
		$V_{(WAKE)}$ = 9 mV; $I_{(WAKE)}$ = 1, RSNS1 = 1, RSNS0 = 1;	–1.4		1.4	
$V_{(WAKE\_TCO)}$	Temperature drift of $V_{(WAKE)}$ accuracy			0.5		%/°C
$t_{(WAKE)}$	Time from application of current and wake of bq34z651			1	10	ms
WATCHDOG TIMER						
t_{WDTINT}	Watchdog start up detect time		250	500	1000	ms
t_{WDWT}	Watchdog detect time		50	100	150	μs
2.5V LDO; $I_{(REG33OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG25)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG25OUT)}$ ≤ 16 mA; T_A = –40°C to 100°C	2.41	2.5	2.59	V
$\Delta V_{(REG25TEMP)}$	Regulator output change with temperature	$I_{(REG25OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2		%
$\Delta V_{(REG25LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG25OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG25LOAD)}$	Load Regulation	0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 2 mA		7	25	mV
		0.2 mA ≤ $I_{(REG25OUT)}$ ≤ 16 mA		25	50	
$I_{(REG25MAX)}$	Current Limit	Drawing current until REG25 = 2 V to 0 V	5	40	75	mA
3.3V LDO; $I_{(REG25OUT)}$ = 0 mA; T_A = 25°C (unless otherwise noted)						
$V_{(REG33)}$	Regulator output voltage	4.5 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ ≤ 25 mA; T_A = –40°C to 100°C	3	3.3	3.6	V
$\Delta V_{(REG33TEMP)}$	Regulator output change with temperature	$I_{(REG33OUT)}$ = 2 mA; T_A = –40°C to 100°C		±0.2		%
$\Delta V_{(REG33LINE)}$	Line regulation	5.4 < VCC or BAT < 25 V; $I_{(REG33OUT)}$ = 2 mA		3	10	mV
$\Delta V_{(REG33LOAD)}$	Load Regulation	0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 2 mA		7	17	mV
		0.2 mA ≤ $I_{(REG33OUT)}$ ≤ 25 mA		40	100	
$I_{(REG33MAX)}$	Current Limit	Drawing current until REG33 = 3 V	25	100	145	mA
		Short REG33 to VSS, REG33 = 0 V	12		65	
THERMISTOR DRIVE						
$V_{(TOUT)}$	Output voltage	$I_{(TOUT)}$ = 0 mA; T_A = 25°C		$V_{(REG25)}$		V
$R_{DS(on)}$	TOUT pass element resistance	$I_{(TOUT)}$ = 1 mA; $R_{DS(on)}$ = ($V_{(REG25)}$ – $V_{(TOUT)}$)/ 1 mA; T_A = –40°C to 100°C		50	100	Ω

ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 μF, $C_{(REG33)}$ = 2.2 μF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED OUTPUTS						
V_{OL}	Output low voltage	LED1, LED2, LED3, LED4, LED5			0.4	V
VCELL+ HIGH VOLTAGE TRANSLATION						
$V_{(VCELL+OUT)}$	Translation output	VC(n) – VC(n+1) = 0 V; T_A = –40°C to 100°C	0.950	0.975	1	V
		VC(n) – VC(n+1) = 4.5 V; T_A = –40°C to 100°C	0.275	0.3	0.375	
$V_{(VCELL+REF)}$		Internal AFE reference voltage; T_A = –40°C to 100°C	0.965	0.975	0.985	
$V_{(VCELL+PACK)}$		Voltage at PACK pin; T_A = –40°C to 100°C	0.98 × $V_{(PACK)}$/18	$V_{(PACK)}$/18	1.02 × $V_{(PACK)}$/18	
$V_{(VCELL+BAT)}$		Voltage at BAT pin; T_A = –40°C to 100°C	0.98 × $V_{(BAT)}$/18	$V_{(BAT)}$/18	1.02 × $V_{(BAT)}$/18	
CMMR	Common mode rejection ratio	VCELL+	40			dB
K	Cell scale factor	K= {VCELL+ output (VC5=0 V; VC4=4.5 V) – VCELL+ output (VC5 = 0 V; VC4 =0 V)}/4.5	0.147	0.150	0.153	
		K= {VCELL+ output (VC2 = 13.5 V; VC1 = 18 V) – VCELL+ output (VC5 = 13.5 V; VC1 = 13.5 V)}/4.5	0.147	0.150	0.153	
$I_{(VCELL+OUT)}$	Drive Current to VCELL+ capacitor	VC(n) – VC(n+1) = 0 V; VCELL+ = 0 V; T_A = –40°C to 100°C	12	18		μA
$V_{(VCELL+O)}$	CELL offset error	CELL output (VC2 = VC1 = 18 V) – CELL output (VC2 = VC1 = 0 V)	–18	–1	18	mV
I_{VCnL}	VC(n) pin leakage current	VC1, VC2, VC3, VC4, VC5 = 3 V	–1	0.01	1	μA
CELL BALANCING						
R_{BAL}	Internal cell balancing FET resistance	$R_{DS(on)}$ for internal FET switch at V_{DS} = 2 V; T_A = 25°C	200	400	600	Ω
HARDWARE SHORT CIRCUIT AND OVERLOAD PROTECTION; T_A = 25°C (unless otherwise noted)						
$V_{(OL)}$	OL detection threshold voltage accuracy	V_{OL} = 25 mV (min)	15	25	35	mV
		V_{OL} = 100 mV; RSNS = 0, 1	90	100	110	
		V_{OL} = 205 mV (max)	185	205	225	
$V_{(SCC)}$	SCC detection threshold voltage accuracy	$V_{(SCC)}$ = 50 mV (min)	30	50	70	mV
		$V_{(SCC)}$ = 200 mV; RSNS = 0, 1	180	200	220	
		$V_{(SCC)}$ = 475 mV (max)	428	475	523	
$V_{(SCD)}$	SCD detection threshold voltage accuracy	$V_{(SCD)}$ = –50 mV (min)	–30	–50	–70	mV
		$V_{(SCD)}$ = –200 mV; RSNS = 0, 1	–180	–200	–220	
		$V_{(SCD)}$ = –475 mV (max)	–428	–475	–523	
t_{da}	Delay time accuracy			±15.25		μs
t_{pd}	Protection circuit propagation delay			50		μs
FET DRIVE CIRCUIT; T_A = 25°C (unless otherwise noted)						
$V_{(DSGON)}$	DSG pin output on voltage	$V_{(DSGON)}$ = $V_{(DSG)}$ – $V_{(PACK)}$; $V_{(GS)}$ = 10 MΩ; DSG and CHG on; T_A = –40°C to 100°C	8	12	16	V
$V_{(CHGON)}$	CHG pin output on voltage	$V_{(CHGON)}$ = $V_{(CHG)}$ – $V_{(BAT)}$; $V_{(GS)}$ = 10 MΩ; DSG and CHG on; T_A = –40°C to 100°C	8	12	16	V
$V_{(DSGOFF)}$	DSG pin output off voltage	$V_{(DSGOFF)}$ = $V_{(DSG)}$ – $V_{(PACK)}$			0.2	V
$V_{(CHGOFF)}$	CHG pin output off voltage	$V_{(CHGOFF)}$ = $V_{(CHG)}$ –$V_{(BAT)}$			0.2	V
t_r	Rise time	C_L= 4700 pF; $V_{(PACK)}$ ≤ DSG ≤ $V_{(PACK)}$ + 4 V		400	1000	μs
		C_L= 4700 pF; $V_{(BAT)}$ ≤ CHG ≤ $V_{(BAT)}$ + 4 V		400	1000	
t_f	Fall time	C_L= 4700 pF; $V_{(PACK)}$ + $V_{(DSGON)}$ ≤ DSG ≤ $V_{(PACK)}$ + 1 V		40	200	μs
		C_L= 4700 pF; $V_{(BAT)}$ + $V_{(CHGON)}$ ≤ CHG ≤ $V_{(BAT)}$ + 1 V		40	200	

ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 μF, $C_{(REG33)}$ = 2.2 μF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(ZVCHG)}$	ZVCHG clamp voltage	BAT = 4.5 V	3.3	3.5	3.7	V
LOGIC; T_A = –40°C to 100°C (unless otherwise noted)						
$R_{(PULLUP)}$	Internal pullup resistance	$\overline{\text{ALERT}}$	60	100	200	kΩ
		$\overline{\text{RESET}}$	1	3	6	
V_{OL}	Logic low output voltage level	$\overline{\text{ALERT}}$			0.2	V
		$\overline{\text{RESET}}$; $V_{(BAT)}$ = 7 V; $V_{(REG25)}$ = 1.5 V; $I_{(RESET)}$ = 200 μA			0.4	
		GPOD; $I_{(GPOD)}$ = 50 μA			0.6	
LOGIC SMBC, SMBD, $\overline{\text{PFIN}}$, $\overline{\text{PRES}}$, SAFE, ALERT, $\overline{\text{DISP}}$						
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	Output voltage high[1]	I_L = –0.5 mA	V_{REG25} – 0.5			V
V_{OL}	Low-level output voltage	$\overline{\text{PRES}}$, $\overline{\text{PFIN}}$, $\overline{\text{ALERT}}$, $\overline{\text{DISP}}$; I_L = 7 mA;			0.4	V
C_I	Input capacitance			5		pF
$I_{(SAFE)}$	SAFE source currents	SAFE active, SAFE = $V_{(REG25)}$ – 0.6 V	–3			mA
$I_{lkg(SAFE)}$	SAFE leakage current	SAFE inactive	–0.2		0.2	μA
I_{lkg}	Input leakage current				1	μA
ADC[2]						
	Input voltage range	TS1, TS2, using Internal V_{ref}	–0.2		1	V
	Conversion time			31.5		ms
	Resolution (no missing codes)		16			bits
	Effective resolution		14	15		bits
	Integral nonlinearity				±0.03	%FSR[3]
	Offset error[4]			140	250	μV
	Offset error drift[4]	T_A = 25°C to 85°C		2.5	18	μV/°C
	Full-scale error[5]			±0.1%	±0.7%	
	Full-scale error drift			50		PPM/°C
	Effective input resistance[6]		8			MΩ
COULOMB COUNTER						
	Input voltage range		–0.20		0.20	V
	Conversion time	Single conversion		250		ms
	Effective resolution	Single conversion	15			bits
	Integral nonlinearity	–0.1 V to 0.20 V		±0.007	±0.034	%FSR
		–0.20 V to –0.1 V		±0.007		
	Offset error [7]	T_A = 25°C to 85°C		10		μV
	Offset error drift			0.4	0.7	μV/°C
	Full-scale error[8] [9]			±0.35%		
	Full-scale error drift			150		PPM/°C
	Effective input resistance[10]	T_A = 25°C to 85°C	2.5			MΩ
INTERNAL TEMPERATURE SENSOR						

(1) RC[0:7] bus
(2) Unless otherwise specified, the specification limits are valid at all measurement speed modes.
(3) Full-scale reference
(4) Post-calibration performance and no I/O changes during conversion with SRN as the ground reference
(5) Uncalibrated performance. This gain error can be eliminated with external calibration.
(6) The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.
(7) Post-calibration performance
(8) Reference voltage for the coulomb counter is typically V_{ref}/3.969 at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(9) Uncalibrated performance. This gain error can be eliminated with external calibration.
(10) The CC input is a switched capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

ELECTRICAL CHARACTERISTICS (continued)

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 μF, $C_{(REG33)}$ = 2.2 μF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TEMP)}$	Temperature sensor voltage(11)			–2.0		mV/°C
VOLTAGE REFERENCE						
	Output voltage		1.215	1.225	1.230	V
	Output voltage drift			65		PPM/°C
HIGH FREQUENCY OSCILLATOR						
$f_{(OSC)}$	Operating frequency			4.194		MHz
$f_{(EIO)}$	Frequency error (12) (13)		–3%	0.25%	3%	
		T_A = 20°C to 70°C	–2%	0.25%	2%	
$t_{(SXO)}$	Start-up time(14)			2.5	5	ms
LOW FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(13) (15)		–2.5%	0.25%	2.5%	
		T_A = 20°C to 70°C	–1.5%	0.25%	1.5%	
$t_{(LSXO)}$	Start-up time(14)				500	μs

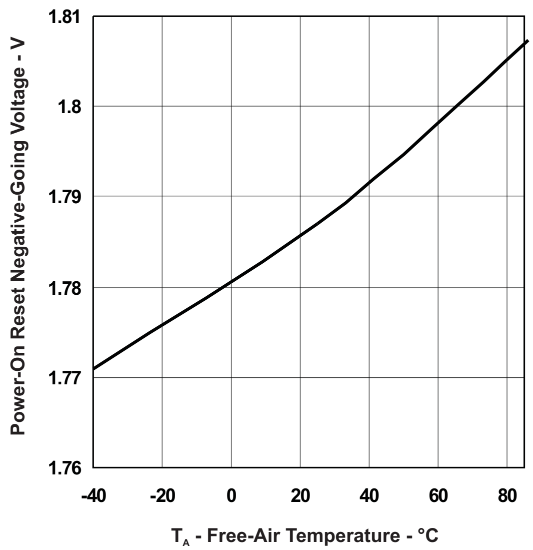
(11) –53.7 LSB/°C
(12) The frequency error is measured from 4.194 MHz.
(13) The frequency drift is included and measured from the trimmed frequency at $V_{(REG25)}$ = 2.5 V, T_A = 25°C.
(14) The startup time is defined as the time it takes for the oscillator output frequency to be ±3%.
(15) The frequency error is measured from 32.768 kHz.

POWER-ON RESET

Over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, $V_{(REG25)}$ = 2.41 V to 2.59 V, $V_{(BAT)}$ = 14 V, $C_{(REG25)}$ = 1 μF, $C_{(REG33)}$ = 2.2 μF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIT–	Negative-going voltage input		1.7	1.8	1.9	V
VHYS	Power-on reset hysteresis		5	125	200	mV
t_{RST}	$\overline{\text{RESET}}$ active low time	Active low time after power up or watchdog reset	100	250	560	μs

POWER ON RESET BEHAVIOR VS FREE-AIR TEMPERATURE



DATA FLASH CHARACTERISTICS OVER RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Typical values at T_A = 25°C and $V_{(REG25)}$ = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data retention	See [1]	10			Years
	Flash programming write-cycles		20k			Cycles
$t_{(ROWPROG)}$	Row programming time				2	ms
$t_{(MASSERASE)}$	Mass-erase time				200	ms
$t_{(PAGEERASE)}$	Page-erase time				20	ms
$I_{(DDPROG)}$	Flash-write supply current			5	10	mA
$I_{(DDERASE)}$	Flash-erase supply current			5	10	mA
RAM/REGISTER BACKUP						
$I_{(RB)}$	RB data-retention input current	$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT-}$, T_A = 85°C		1000	2500	nA
		$V_{(RBI)} > V_{(RBI)MIN}$, $V_{REG25} < V_{IT-}$, T_A = 25°C		90	220	
$V_{(RB)}$	RB data-retention input voltage[1]		1.7			V

(1) Specified by design. Not production tested.

SMBus TIMING CHARACTERISTICS

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

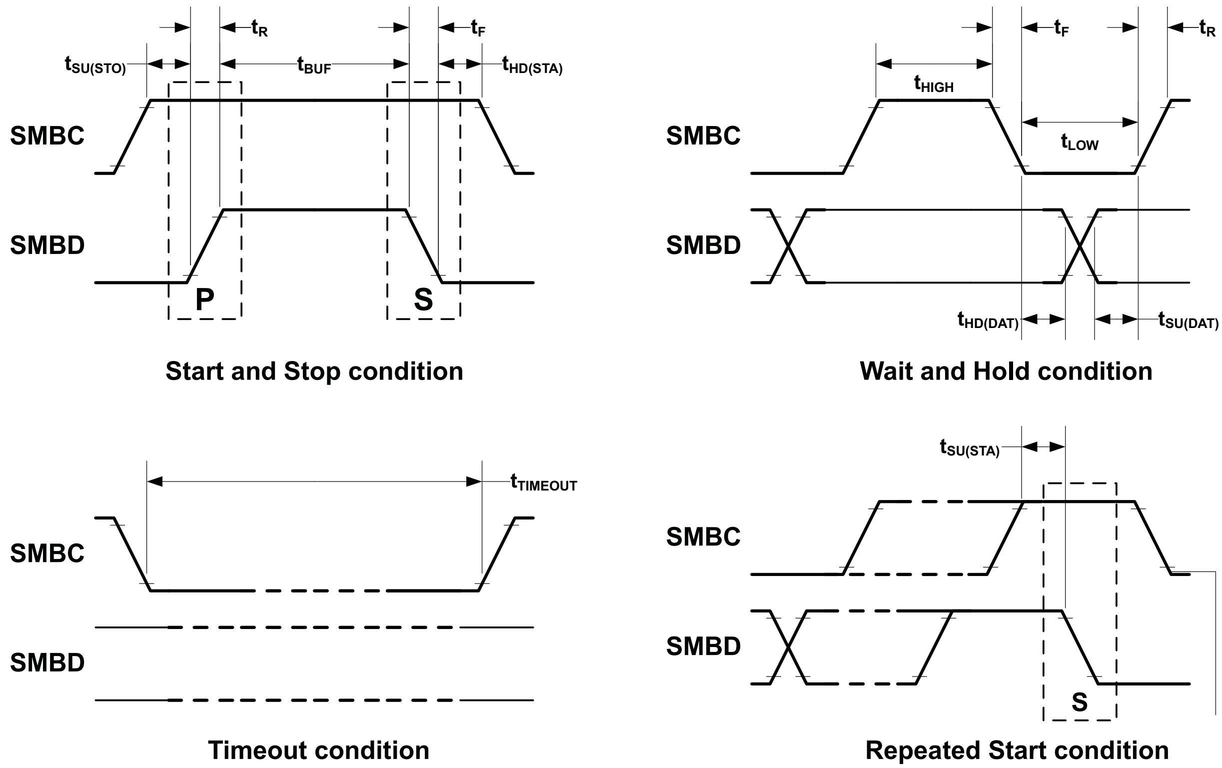
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(SMB)}$	SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz

SMBus TIMING CHARACTERISTICS (continued)

T_A = –40°C to 85°C Typical Values at T_A = 25°C and V_{REG25} = 2.5 V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(MAS)}$	SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
$t_{(BUF)}$	Bus free time between start and stop (See Figure 1.)		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start (See Figure 1.)		4			µs
$t_{(SU:STA)}$	Repeated start setup time (See Figure 1.)		4.7			µs
$t_{(SU:STO)}$	Stop setup time (See Figure 1.)		4			µs
$t_{(HD:DAT)}$	Data hold time (See Figure 1.)	Receive mode	0			ns
		Transmit mode	300			
$t_{(SU:DAT)}$	Data setup time (See Figure 1.)		250			ns
$t_{(TIMEOUT)}$	Error signal/detect (See Figure 1.)	See (1)	25		35	µs
$t_{(LOW)}$	Clock low period (See Figure 1.)		4.7			µs
$t_{(HIGH)}$	Clock high period (See Figure 1.)	See (2)	4		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
$t_{(LOW:MEXT)}$	Cumulative clock low master extend time (See Figure 1.)	See (4)			10	ms
t_f	Clock/data fall time	See (5)			300	ns
t_r	Clock/data rise time	See (6)			1000	ns

(1) The bq34z651 times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving bq34z651 that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0]=0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) $t_{(LOW:MEXT)}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.
(5) Rise time t_r = VILMAX – 0.15) to (VIHMIN + 0.15)
(6) Fall time t_f = 0.9V_{DD} to (VILMAX – 0.15)



A. SCLKACK is the acknowledge-related clock pulse generated by the master.

Figure 1. SMBus Timing Diagram

FEATURE SET

Primary (1st Level) Safety Features

The bq34z651 supports a wide range of battery and system protection features that can be easily configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq34z651 can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- 2nd-level protection IC input
- Safety overcurrent in charge and discharge
- Safety over-temperature in charge and discharge with independent alarms and thresholds for each thermistor
- Charge FET and zero-volt charge FET fault
- Discharge FET fault
- Cell imbalance detection (active and at rest)
- Open thermistor detection
- Fuse blow detection
- AFE communication fault

Charge Control Features

The bq34z651 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges, and for varying the charging current according to the cell voltage
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Determines the chemical state of charge of each battery cell using Impedance Track, and can reduce the charge difference of the battery cells in a fully charged state of the battery pack, gradually using the cell balancing algorithm during charging. This prevents fully charged cells from overcharging and causing excessive degradation and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms
- Battery heater control to allow battery charging in low ambient temperatures

Gas Gauging

The bq34z651 uses the Impedance Track Technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge discharge learning cycle required.

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note (SLUA364) for further details.

Lifetime Data Logging Features

The bq34z651 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored include:

- Lifetime maximum temperature
- Lifetime maximum temperature count
- Lifetime maximum temperature duration
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime maximum battery cell voltage count
- Lifetime maximum battery cell voltage duration
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average discharge current
- Lifetime maximum average discharge power
- Lifetime average temperature

Authentication

The bq34z651 supports authentication by the host using SHA-1.

Power Modes

The bq34z651 supports three different power modes to reduce power consumption:

- In Normal Mode, the bq34z651 performs measurements, calculations, protection decisions and data updates in 1-second intervals. Between these intervals, the bq34z651 is in a reduced power stage.
- In Sleep Mode, the bq34z651 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq34z651 is in a reduced power stage. The bq34z651 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In Shutdown Mode, the bq34z651 is completely disabled.

CONFIGURATION

Oscillator Function

The bq34z651 fully integrates the system oscillators; therefore, no external components are required for this feature.

System Present Operation

The bq34z651 periodically verifies the $\overline{PRES}$ pin and detects that the battery is present in the system via a low state on a $\overline{PRES}$ input. When this occurs, the bq34z651 enters normal operating mode. When the pack is removed from the system and the $\overline{PRES}$ input is high, the bq34z651 enters the battery-removed state, disabling the charge, discharge, and ZVCHG FETs. The $\overline{PRES}$ input is ignored and can be left floating when non-removal mode is set in the data flash.

BATTERY PARAMETER MEASUREMENTS

The bq34z651 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from –0.25 V to 0.25 V. The bq34z651 detects charge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when $V_{SR} = V_{(SRP)} – V_{(SRN)}$ is negative. The bq34z651 continuously integrates the signal over time using an internal counter. The fundamental rate of the counter is 0.65 nVh.

Voltage

The bq34z651 updates the individual series cell voltages at one second intervals. The internal ADC of the bq34z651 measures the voltage, and scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas-gauging.

Current

The bq34z651 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a 5-mΩ to 20-mΩ typ. sense resistor.

Wake Function

The bq34z651 can exit sleep mode, if enabled, by the presence of a programmable level of current signal across SRP and SRN.

Auto Calibration

The bq34z651 provides an auto-calibration feature to cancel the voltage offset error across SRN and SRP for maximum charge measurement accuracy. The bq34z651 performs auto-calibration when the SMBus lines stay low continuously for a minimum of a programmable amount of time.

Temperature

The bq34z651 has an internal temperature sensor and two external temperature sensor inputs, TS1 and TS2, used in conjunction with two identical NTC thermistors (default is Semitec 103AT) to sense the battery environmental temperature. The bq34z651 can be configured to use the internal temperature sensor or up to two external temperature sensors.

COMMUNICATIONS

The bq34z651 uses SMBus v1.1 with Master Mode and packet error checking (PEC) options per the SBS specification.

SMBus On and Off State

The bq34z651 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

SBS Commands

Table 2. SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	Hex	2	0x0000	0xffff	—	—
0x01	R/W	RemainingCapacityAlarm	Integer	2	0	700 or 1000	300 or 432	mAh or 10 mWh
0x02	R/W	RemainingTimeAlarm	Unsigned integer	2	0	30	10	min
0x03	R/W	BatteryMode	Hex	2	0x0000	0xffff	—	—
0x04	R/W	AtRate	Integer	2	–32,768	32,767	—	mA or 10 mW
0x05	R	AtRateTimeToFull	Unsigned integer	2	0	65,535	—	min
0x06	R	AtRateTimeToEmpty	Unsigned integer	2	0	65,535	—	min
0x07	R	AtRateOK	Unsigned integer	2	0	65,535	—	—
0x08	R	Temperature	Unsigned integer	2	0	65,535	—	0.1°K
0x09	R	Voltage	Unsigned integer	2	0	20,000	—	mV
0x0a	R	Current	Integer	2	–32,768	32767	—	mA
0x0b	R	AverageCurrent	Integer	2	–32,768	32,767	—	mA
0x0c	R	MaxError	Unsigned integer	1	0	100	—	%
0x0d	R	RelativeStateOfCharge	Unsigned integer	1	0	100	—	%
0x0e	R	AbsoluteStateOfCharge	Unsigned integer	1	0	100+	—	%
0x0f	R/W	RemainingCapacity	Unsigned integer	2	0	65,535	—	mAh or 10 mWh
0x10	R	FullChargeCapacity	Unsigned integer	2	0	65,535	—	mAh or 10 mWh
0x11	R	RunTimeToEmpty	Unsigned integer	2	0	65,534	—	min
0x12	R	AverageTimeToEmpty	Unsigned integer	2	0	65,534	—	min
0x13	R	AverageTimeToFull	Unsigned integer	2	0	65,534	—	min
0x14	R	ChargingCurrent	Unsigned integer	2	0	65,534	—	mA
0x15	R	ChargingVoltage	Unsigned integer	2	0	65,534	—	mV
0x16	R	BatteryStatus	Hex	2	0x0000	0xdbff	—	—
0x17	R/W	CycleCount	Unsigned integer	2	0	65,535	0	—
0x18	R/W	DesignCapacity	Integer	2	0	32,767	4400 or 6336	mAh or 10 mWh
0x19	R/W	DesignVoltage	Integer	2	7000	18,000	14,400	mV

Table 2. SBS COMMANDS (continued)

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x1a	R/W	SpecificationInfo	Hex	2	0x0000	0xffff	0x0031	—
0x1b	R/W	ManufactureDate	Unsigned integer	2	0	65,535	0	—
0x1c	R/W	SerialNumber	Hex	2	0x0000	0xffff	0x0000	—
0x20	R/W	ManufacturerName	String	20+1	—	—	Texas Instruments	—
0x21	R/W	DeviceName	String	20+1	—	—	bq34z651	—
0x22	R/W	DeviceChemistry	String	4+1	—	—	LION	—
0x23	R	ManufacturerData	String	14+1	—	—	—	—
0x2f	R/W	Authenticate	String	20+1	—	—	—	—
0x3c	R	CellVoltage4	Unsigned integer	2	0	65,535	—	mV
0x3d	R	CellVoltage3	Unsigned integer	2	0	65,535	—	mV
0x3e	R	CellVoltage2	Unsigned integer	2	0	65,535	—	mV
0x3f	R	CellVoltage1	Unsigned integer	2	0	65,535	—	mV

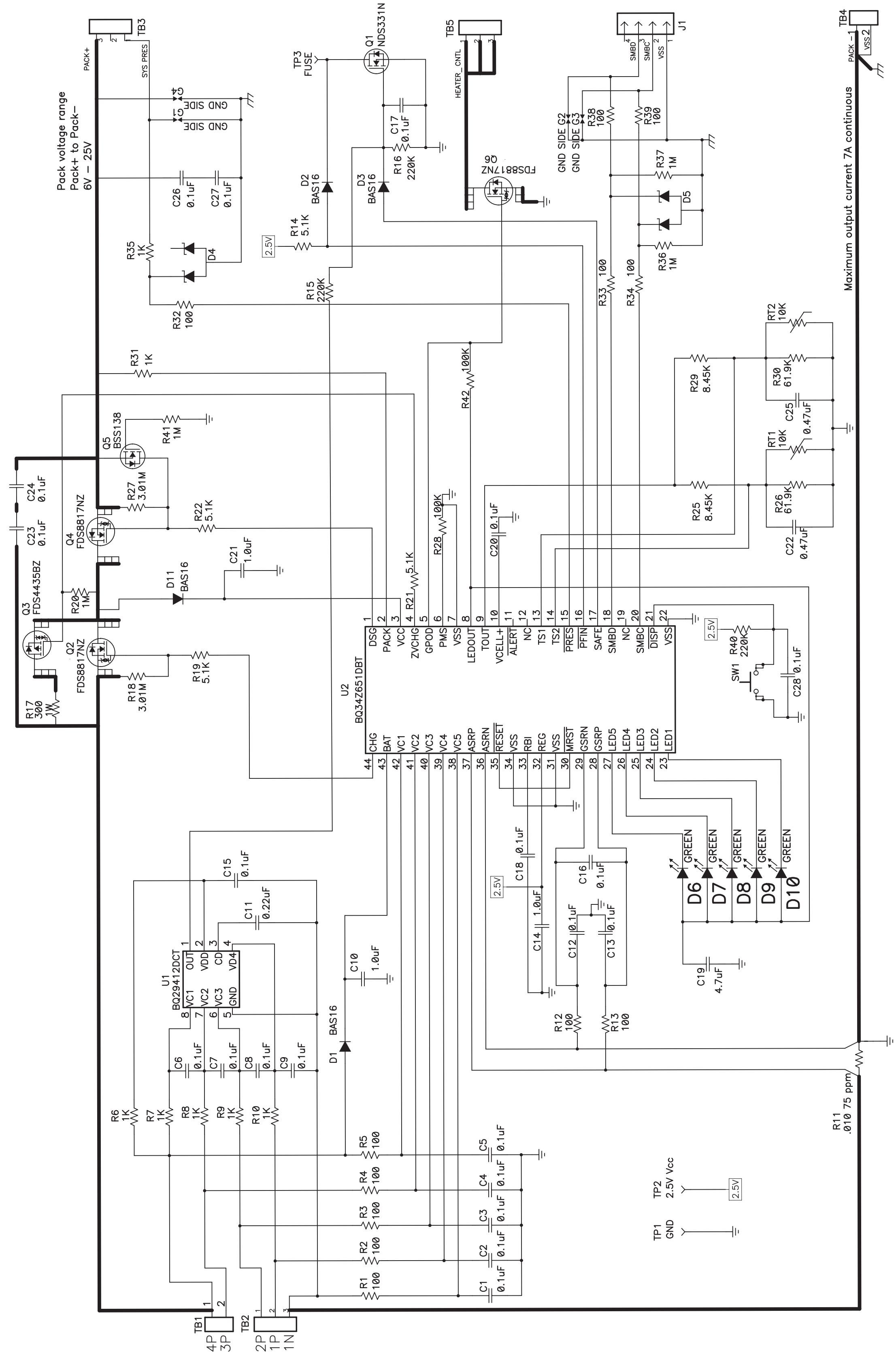
Table 3. EXTENDED SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x45	R	AFEData	String	11+1	—	—	—	—
0x46	R/W	FETControl	Hex	2	0x00	0xff	—	—
0x4f	R	StateOfHealth	Hex	2	0x0000	0xffff	—	%
0x51	R	SafetyStatus	Hex	2	0x0000	0xffff	—	—
0x52	R	PFAlert	Hex	2	0x0000	0xffff	—	—
0x53	R	PFStatus	Hex	2	0x0000	0xffff	—	—
0x54	R	OperationStatus	Hex	2	0x0000	0xffff	—	—
0x55	R	ChargingStatus	Hex	2	0x0000	0xffff	—	—
0x57	R	ResetData	Hex	2	0x0000	0xffff	—	—
0x58	R	WDResetData	Unsigned integer	2	0	65,535	—	—
0x5a	R	PackVoltage	Unsigned integer	2	0	65,535	—	mV
0x5d	R	AverageVoltage	Unsigned integer	2	0	65,535	—	mV
0x5e	R	TS1Temperature	Integer	2	–400	1200	—	0.1°C
0x5f	R	TS2Temperature	Integer	2	–400	1200	—	0.1°C
0x60	R/W	UnSealKey	Hex	4	0x00000000	0xffffffff	—	—
0x61	R/W	FullAccessKey	Hex	4	0x00000000	0xffffffff	—	—
0x62	R/W	PFKey	Hex	4	0x00000000	0xffffffff	—	—
0x63	R/W	AuthenKey3	Hex	4	0x00000000	0xffffffff	—	—
0x64	R/W	AuthenKey2	Hex	4	0x00000000	0xffffffff	—	—
0x65	R/W	AuthenKey1	Hex	4	0x00000000	0xffffffff	—	—
0x66	R/W	AuthenKey0	Hex	4	0x00000000	0xffffffff	—	—
0x68	R	SafetyAlert2	Hex	2	0x0000	0x000f	—	—
0x69	R	SafetyStatus2	Hex	2	0x0000	0x000f	—	—
0x6a	R	PFAlert2	Hex	2	0x0000	0x000f	—	—
0x6b	R	PFStatus2	Hex	2	0x0000	0x000f	—	—

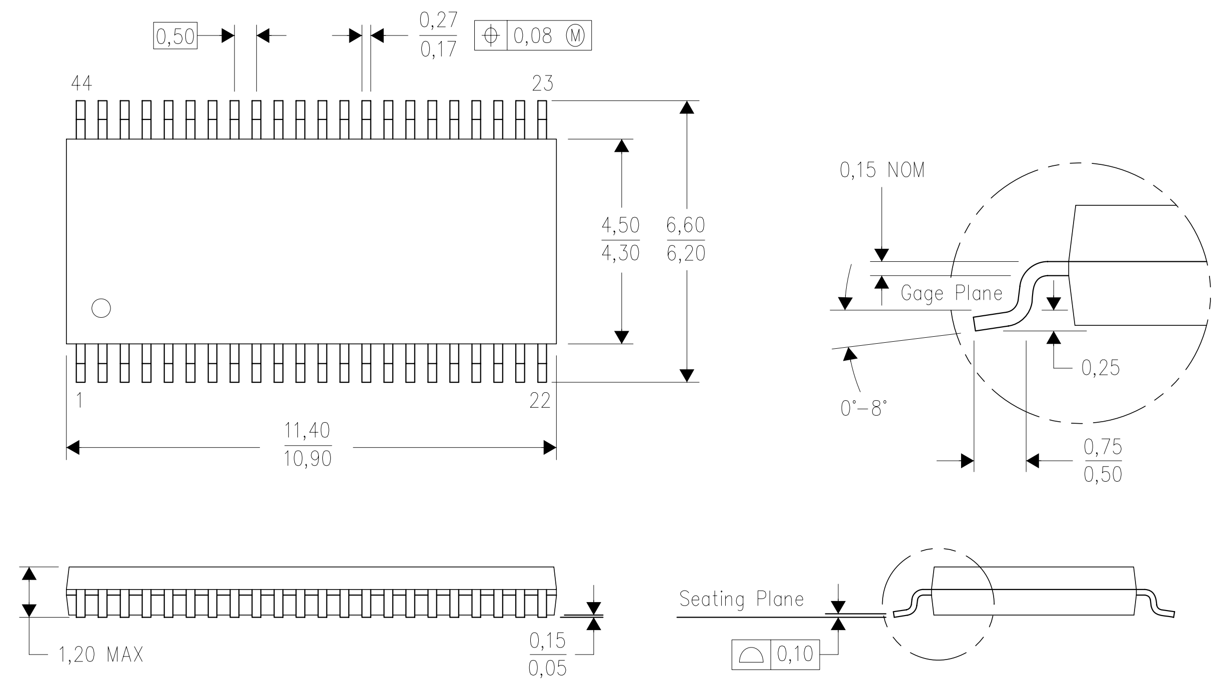
Table 3. EXTENDED SBS COMMANDS (continued)

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x6c	R	ManufBlock1	String	20	—	—	—	—
0x6d	R	ManufBlock2	String	20	—	—	—	—
0x6e	R	ManufBlock3	String	20	—	—	—	—
0x6f	R	ManufBlock4	String	20	—	—	—	—
0x70	R/W	ManufacturerInfo	String	31+1	—	—	—	—
0x71	R/W	SenseResistor	Unsigned integer	2	0	65,535	—	μΩ
0x72	R	TempRange	Hex	2	—	—	—	—
0x73	R	LifetimeData1	String	32+1	—	—	—	—
0x74	R	LifetimeData2	String	8+1	—	—	—	—
0x77	R/W	DataFlashSubClassID	Hex	2	0x0000	0xffff	—	—
0x78	R/W	DataFlashSubClassPage1	Hex	32	—	—	—	—
0x79	R/W	DataFlashSubClassPage2	Hex	32	—	—	—	—
0x7a	R/W	DataFlashSubClassPage3	Hex	32	—	—	—	—
0x7b	R/W	DataFlashSubClassPage4	Hex	32	—	—	—	—
0x7c	R/W	DataFlashSubClassPage5	Hex	32	—	—	—	—
0x7d	R/W	DataFlashSubClassPage6	Hex	32	—	—	—	—
0x7e	R/W	DataFlashSubClassPage7	Hex	32	—	—	—	—
0x7f	R/W	DataFlashSubClassPage8	Hex	32	—	—	—	—

APPLICATION SCHEMATIC



DBT (R–PDSO–G44) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ34Z651DBT	ACTIVE	TSSOP	DBT	44	40	RoHS & Green	NIPDAU	Level-2-250C-1 YEAR	-40 to 85	BQ34Z651	Samples
BQ34Z651DBTR	ACTIVE	TSSOP	DBT	44	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ34Z651	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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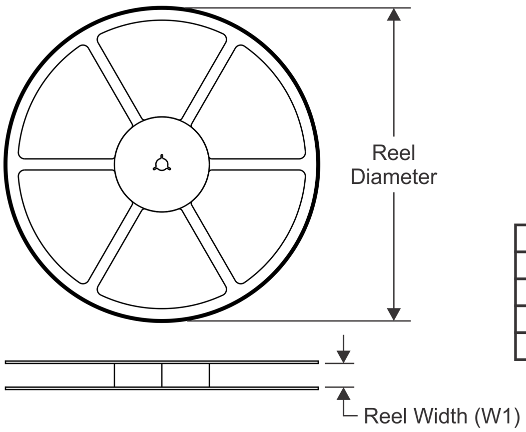
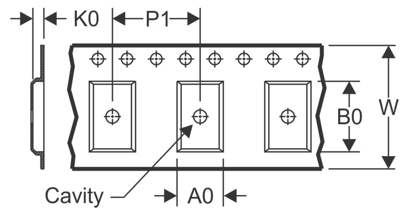
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

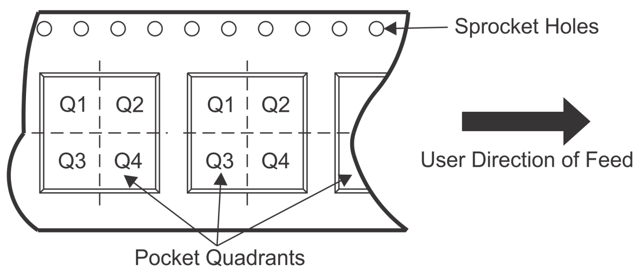


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

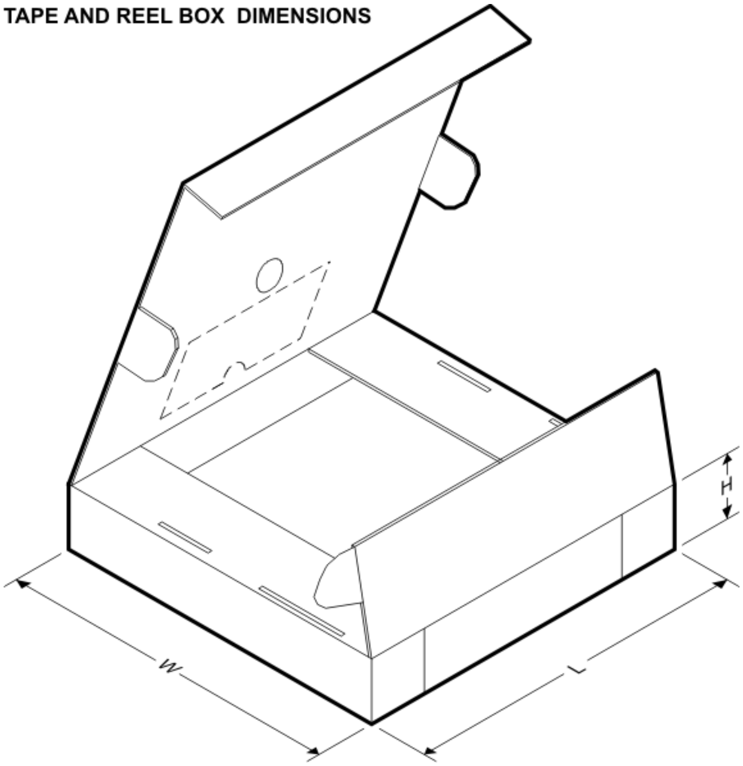
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ34Z651DBTR	TSSOP	DBT	44	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1

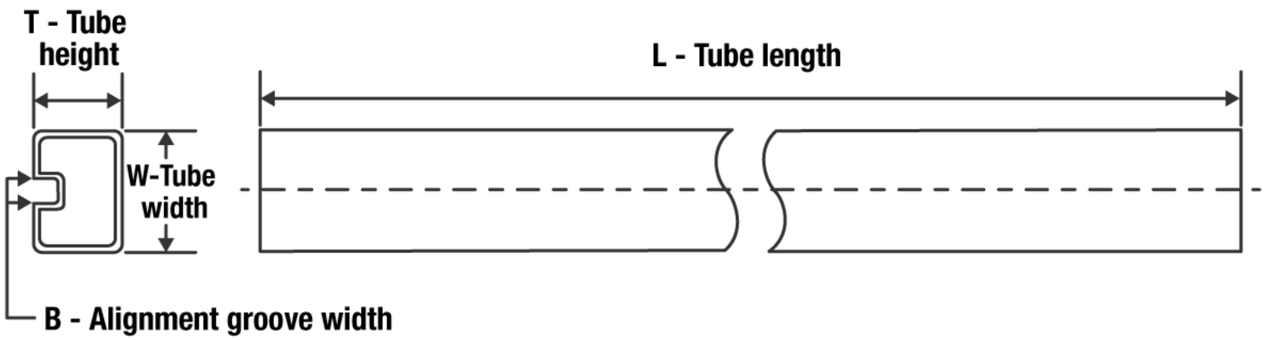
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

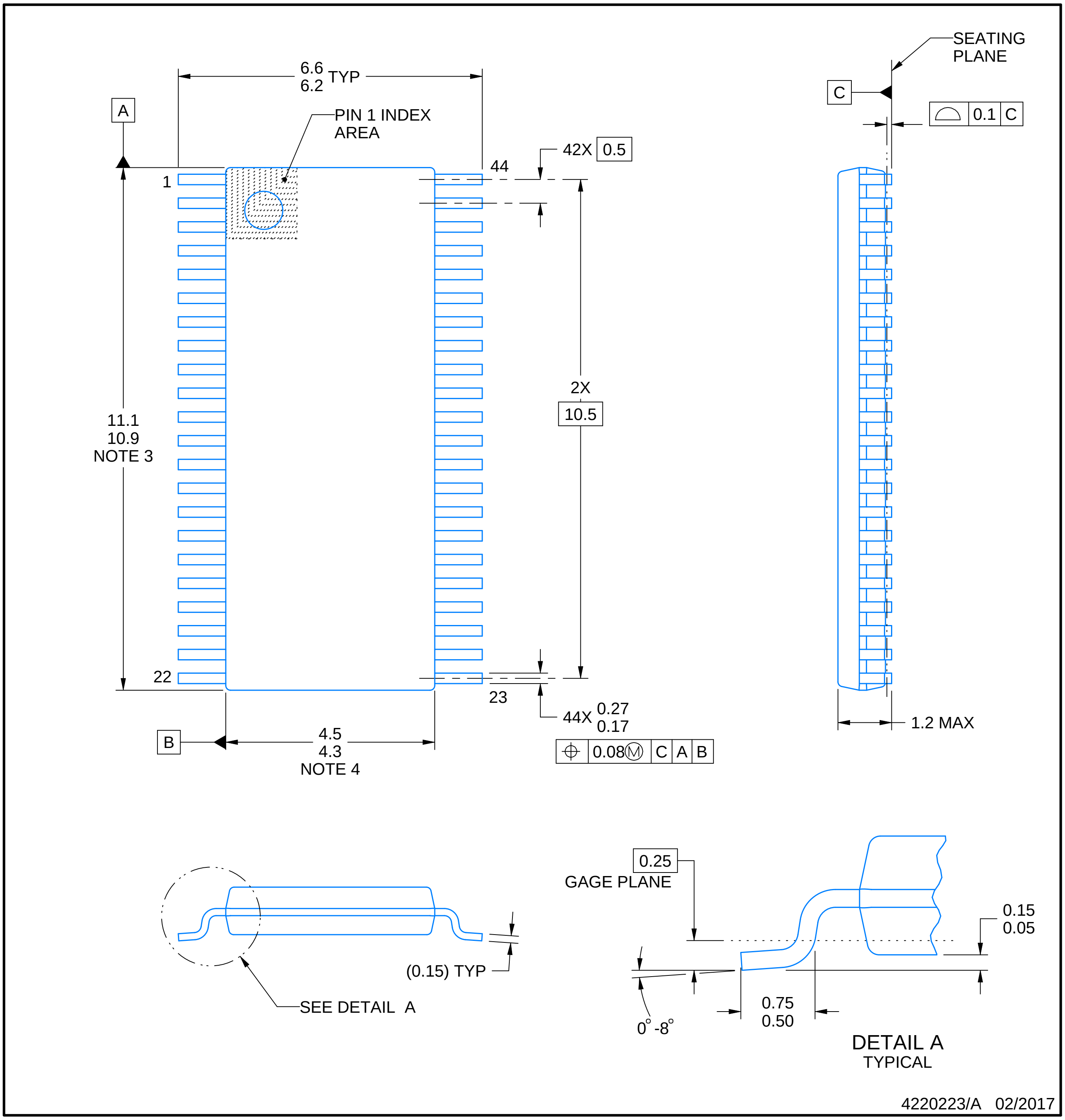
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ34Z651DBTR	TSSOP	DBT	44	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ34Z651DBT	DBT	TSSOP	44	40	530	10.2	3600	3.5



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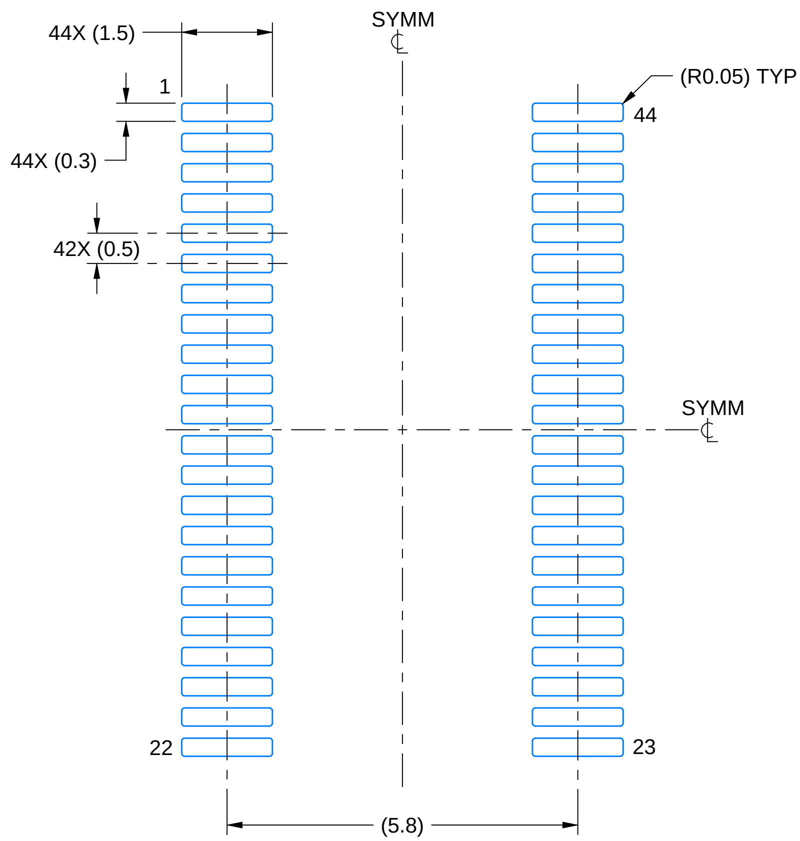
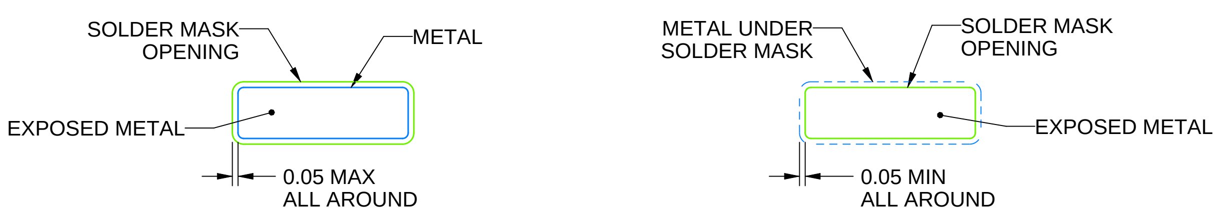
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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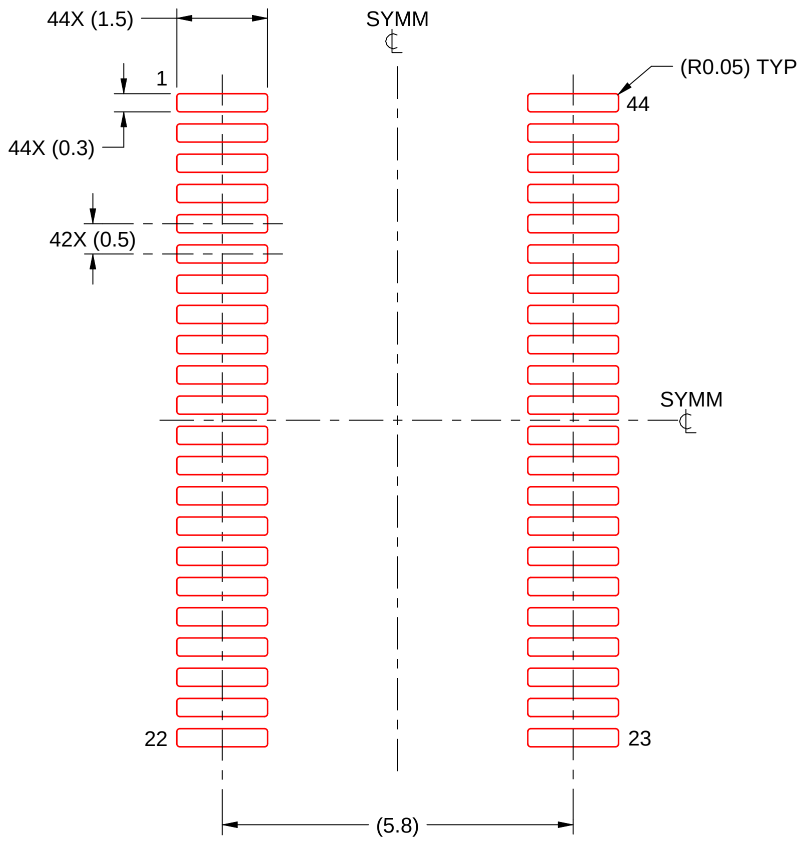
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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