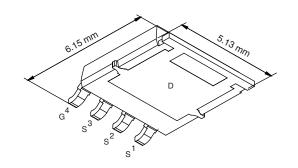




# N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)			
40	$0.0095 \text{ at V}_{GS} = 10 \text{ V}$	20 <sup>a</sup>	16 nC			
	$0.0115$ at $V_{GS} = 4.5 \text{ V}$	20 <sup>a</sup>	10110			

#### PowerPAK® SO-8L Single



Ordering Information: SiJ800DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### **FEATURES**

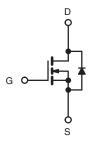
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



ROHS COMPLIANT HALOGEN FREE

#### **APPLICATIONS**

- · Backlight Inverter
- High-Side Switch
- · Server, VRM, POL
- DC/DC



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	40	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	I <sub>D</sub>	20 <sup>a</sup> 20 <sup>a</sup> 15.6 <sup>b, c</sup> 12.5 <sup>b, c</sup>	Α	
Pulsed Drain Current Avalanche Current	L = 0.1 mH	I <sub>DM</sub>	80 30		
Avalanche Energy	L = U.1 IIII	E <sub>AS</sub>	45	mJ	
Continuous Source-Drain Diode Current $ T_C = 25  ^{\circ}\text{C} $ $ T_A = 25  ^{\circ}\text{C} $		- I <sub>S</sub>	20 <sup>a</sup> 3.5 <sup>b, c</sup>	Α	
Maximum Power Dissipation	$T_{C} = 25 ^{\circ}\text{C}$ $T_{C} = 70 ^{\circ}\text{C}$ $T_{A} = 25 ^{\circ}\text{C}$ $T_{A} = 70 ^{\circ}\text{C}$	P <sub>D</sub>	35.7 22.9 4.2 <sup>b, c</sup> 2.7 <sup>b, c</sup>	w	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	$R_{thJA}$	25	30	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	2.9	3.5		

#### Notes:

- a. Based on  $T_C$  = 25 °C. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (<a href="www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 70 °C/W.

# SiJ800DP

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1. 10 1		44		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 1.0 mA		- 5.9			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.2		3	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μΑ	
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0078	0.0095	Ω	
	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$		0.0092	0.0115		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		70		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			2400			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		260		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			100			
Total Gate Charge		$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	$V_1$ , $V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$ 37	37	56	nC	
				16	24		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$		6.5			
Gate-Drain Charge	$Q_{gd}$			4.5			
Gate Resistance	$R_g$	f = 1 MHz	1	5	10	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			30	45	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 20 $\Omega$		15	25		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1.0 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1.0 \Omega$		45	70		
Fall Time	t <sub>f</sub>			15	25		
Turn-On Delay Time	t <sub>d(on)</sub>			9	15		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 20 V, $R_L$ = 20 $\Omega$		5	10		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1.0 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		40	60		
Fall Time	t <sub>f</sub>			5	10		
<b>Drain-Source Body Diode Characteristi</b>	cs			•			
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			20	Δ	
Pulse Diode Forward Current	I <sub>SM</sub>				80	_ A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 3.5 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			22	35	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	$I_F = 20 \text{ A, dl/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		14	25	nC	
Reverse Recovery Fall Time	t <sub>a</sub>			11			
Reverse Recovery Rise Time	t <sub>b</sub>			11		ns	

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

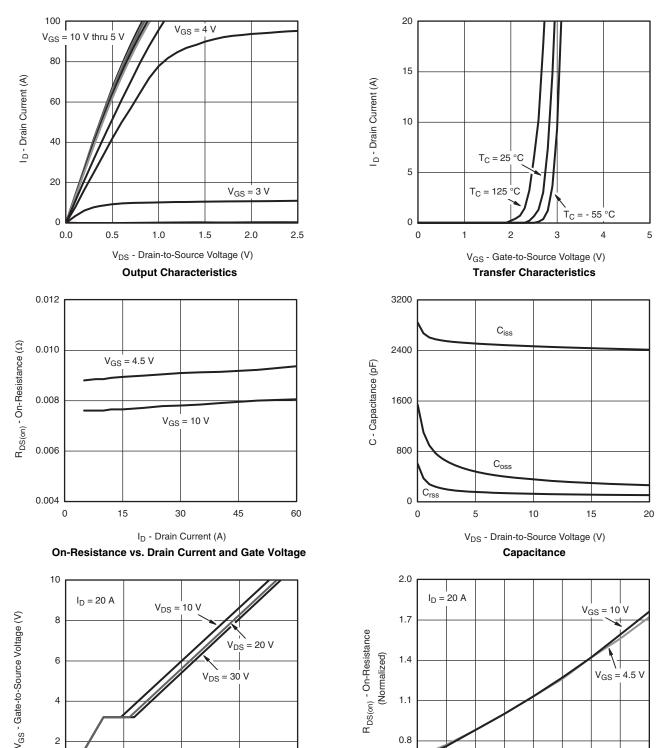
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.







# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $\begin{array}{ccc} \textbf{Q}_{g} \text{ - Total Gate Charge (nC)} & \textbf{T}_{J} \text{ - Junction Temperature (°C)} \\ \textbf{Gate Charge} & \textbf{On-Resistance vs. Junction Temperature} \end{array}$ 

40

0.5

- 50

- 25

0

25

50

75

100

0

20

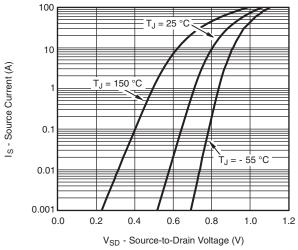
10

125 150

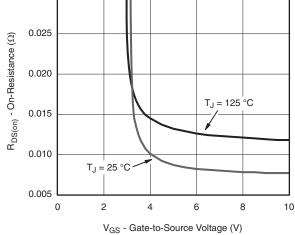
# Vishay Siliconix

# VISHAY.

# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

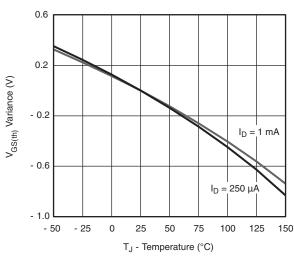


Source-Drain Diode Forward Voltage

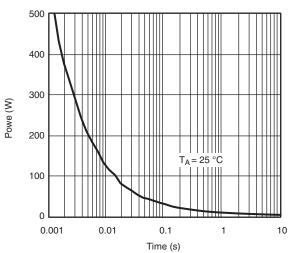


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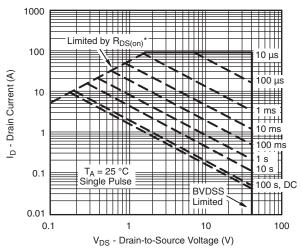
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



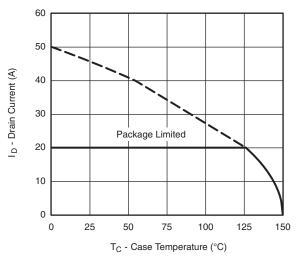
\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

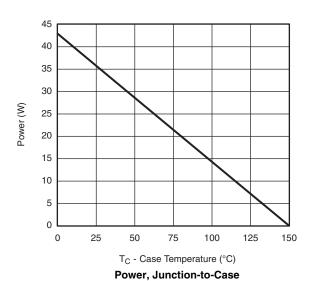


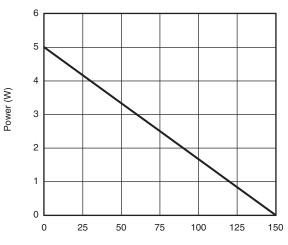


### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



#### **Current Derating\***





T<sub>A</sub> - Ambient Temperature (°C) **Power, Junction-to-Ambient** 

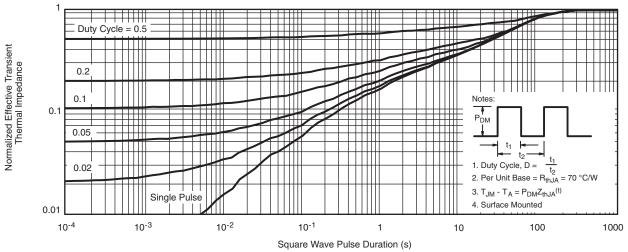
Document Number: 64803 S09-0668-Rev. A, 20-Apr-09

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

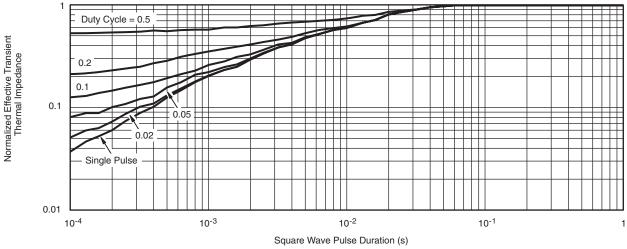
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# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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