PCN Number:		201412030	000				PCN Dat	e:	12/04/2014
Title: TPS2592AA/B/Z Datasl			et c	hange					
Customer Contact:		PCN Manager		Phone: +1(214) 480-6037		37	Dept: Qua		ality Services
Change	Туре:								
Asse	embly Site			Design			Wafer Bump Site		
Asse	embly Process		\boxtimes	Data Sh	eet		Wafer Bump Material		
Asse	embly Materia	s		Part nun	nber change		Wafer Bump Process		p Process
Mechanical Specification			Test Site	9		Wafer I	Fab S	Site	
Pacl	king/Shipping/	Labeling		Test Pro	cess		Wafer Fab Materials		
							Wafer I	Fab I	Process

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification, etc.

The product datasheet(s) is being updated to Split the datasheet into A, B, Z versions and reduce the current limit ranges.

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS2592AA/AL	SLVSC11B	SLVSC11C
TPS2592BA/BL	SLVSC11B	SLVSCU2
TPS2592ZA/ZL	SLVSC11B	SLVSCU3

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/tps2592aa?qgpn=tps2592aa http://www.ti.com/product/tps2592ba?qgpn=tps2592ba http://www.ti.com/product/tps2592za?qgpn=tps2592za

The following section provides further details on specification changes.

Texas INSTRUMENTS

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TPS2592AA, TPS2592AL SLVSC11C - JUNE 2013-REVISED DECEMBER 2014

Primary Spec Changes from Revision B (2013) to Revision C

Page

 Added Maximum power dissipation in Absolute Maximum Ratings..... ΜΔΧ UNIT

Maximum power dissipation ⁽³⁾ , P _D	$T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C$		40	W		
$= (V_{IN} - V_{OUT}) \times I_{OUT}$	$T_A = 0^{\circ}C$ to +85 $^{\circ}C$		50	vv		
(3) Refer detailed explanation in the application section Maximum Device Power Dissipation Considerations						

on section Maximum Device Power Dissipation Considerations ed explanation in the appl

Change From: (page 3)

 Changed Con 	Changed Continuous output current and Change Resistance values					
		MIN	түр	MAX	UNIT	
Continuos output current	lout	0		5	Α	
Resistance	ILIM	40.2	100	162	kΩ	

Change To: (page 5)

			MIN	TYP MAX	UNIT
Continuous output current		$T_A = -40^{\circ}C$ to +85°C	0	2.8	^
	OUT	$T_A = 0^{\circ}C$ to +85°C	0	3.4	A
Registeres	ILIM	T _A = -40°C to +85°C	10	80.6	kΩ
Resistance		$T_A = 0^{\circ}C$ to +85°C	10	100	KΩ

Updated (page 23)

10.3 Maximum Device Power Dissipation Considerations

To prevent damage to the TPS2592x, it is necessary to keep internal power dissipation (P_D) below the levels specified in below Table. The power dissipation is defined as $(P_D = (V_{IN} - V_{OUT}) \times I_{OUT})$.

During normal operation P_D is low (typically < ½ Watt) because the FET is fully on with low (V_{IN} - V_{OUT}). However, during short circuit and surge protection the FET may be only partially on and $(V_{IN} - V_{OUT})$ can be high.

Example 1: Short Circuit on Output \rightarrow VIN = 12 V, I_{LIMIT} = 3 A. T_J = -40°C

• P_D = 12 V x 3 A = 36 W

• $OK \rightarrow (P_D = 36 \text{ W}) < (P_{D_MAX} = 40 \text{ W})$

Example 2: Short Circuit on Output
$$\rightarrow$$
 VIN = 13.2 V, I_{LIMIT} = 3.7 A

• P_D = 13.2 V x 3.7 A = 49 W

• OK at $T_J = 0^{\circ}C \rightarrow (P_D = 49 \text{ W}) < (P_{D_MAX} \text{ at } 0^{\circ}C = 50 \text{ W})$

• NOT OK at $T_J = -40^{\circ}C \rightarrow (P_D = 51 \text{ W}) > (P_{D_MAX} \text{ at } -40^{\circ}C = 40 \text{ W})$

Example 3: Surge Clamp VIN = 12 V, I_{LIMIT} = 3 A. T_J = 0°C, V_{SURGE} =19 V, V_{CLAMP} = 15 V

• P_D = (19 – 15) x 3 A = 12 Watt

• OK at
$$0^{\circ}C \rightarrow (PD = 12 \text{ W}) < (PD_MAX \text{ at } 0^{\circ}C = 50 \text{ W})$$

5 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release

Primary Spec Changes

Page

Added Maximum power dissipation in Absolute Maximum Ratings						
		MIN	MAX	UNIT		
Maximum power dissipation ⁽³⁾ , P _D	$T_{\rm A} = -40^{\circ}$ C to +85 °C		40	W		
$= (V_{IN} - V_{OUT}) \times I_{OUT}$	$T_{A} = 0^{\circ}C \text{ to } +85^{\circ}C$		50	vv		

(3) Refer detailed explanation in the application section Maximum Device Power Dissipation Considerations

Updated (page 23)

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During normal operation P_D is low (typically < 1/2 Watt) because the FET is fully on with low (V_{IN} – V_{OUT}). However, during short circuit and surge protection the FET may be only partially on and (VIN - VOUT) can be high. $= 12 \text{ V}, \text{ I}_{\text{LIMIT}} = 3 \text{ A}. \text{ T}_{\text{J}} = -40^{\circ}\text{C}$

Example 1: Short Circuit on Output
$$\rightarrow$$
 VIN :
• P₂ = 12 V × 3 A = 36 W

•
$$P_D = 12 \vee X 3 A = 30 \vee V$$

• OK \rightarrow (P_D = 36 W) < (P_{D_MAX} = 40 W)

Example 2: Short Circuit on Output \rightarrow VIN = 13.2 V, I_{LIMIT} = 3.7 A

• P_D = 13.2 V x 3.7 A = 49 W

• OK at $T_J = 0^{\circ}C \rightarrow (P_D = 49 \text{ W}) < (P_{D_MAX} \text{ at } 0^{\circ}C = 50 \text{ W})$

• NOT OK at $T_J = -40^{\circ}C \rightarrow (P_D = 51 \text{ W}) > (P_{D_MAX} \text{ at } -40^{\circ}C = 40 \text{ W})$

Example 3: Surge Clamp VIN = 12 V, I_{LIMIT} = 3 A. T_J = 0°C, V_{SURGE} =19 V, V_{CLAMP} = 15 V

• P_D = (19 – 15) x 3 A = 12 Watt

• OK at $0^{\circ}C \rightarrow (PD = 12 \text{ W}) < (PD_MAX \text{ at } 0^{\circ}C = 50 \text{ W})$



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5 Revision History

DATE	REVISION	NOTES
December 2014	*	Initial release

Primary Spec Changes

TEXAS INSTRUMENTS

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• Added Maximum power dissipation in Absolute Maximum Ratings..... ΜΔΧ MIN Т LINIT

			1117 121	0			
Maximum power dissipation ⁽³⁾ , P _D	$T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C$		40	W			
$= (V_{IN} - V_{OUT}) \times I_{OUT}$	$T_A = 0^{\circ}C$ to +85 $^{\circ}C$		50	vv			
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er detailed explanation ir (3)app

Updated (page 23)

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During normal operation P_D is low (typically < $\frac{1}{2}$ Watt) because the FET is fully on with low (V_{IN} - V_{OUT}). However, during short circuit and surge protection the FET may be only partially on and (VIN - VOUT) can be high.

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• $OK \rightarrow (P_D = 36 \text{ W}) < (P_{D_MAX} = 40 \text{ W})$

Example 2: Short Circuit on Output \rightarrow VIN = 13.2 V, I_{LIMIT} = 3.7 A

• P_D = 13.2 V x 3.7 A = 49 W

• OK at $T_J = 0^{\circ}C \rightarrow (P_D = 49 \text{ W}) < (P_{D_MAX} \text{ at } 0^{\circ}C = 50 \text{ W})$

• NOT OK at $T_J = -40^{\circ}C \rightarrow (P_D = 51 \text{ W}) > (P_{D_MAX} \text{ at } -40^{\circ}C = 40 \text{ W})$

Example 3: Surge Clamp VIN = 12 V, I_{LIMIT} = 3 A. T_J = 0°C, V_{SURGE} =19 V, V_{CLAMP} = 15 V

• $P_D = (19 - 15) \times 3 A = 12 Watt$

• OK at $0^{\circ}C \rightarrow (PD = 12 \text{ W}) < (PD_MAX \text{ at } 0^{\circ}C = 50 \text{ W})$

Change From: (page 3)

 Changed Con 	Changed Continuous output current and Change Resistance values					
		MIN	түр	MAX	UNIT	
Continuos output current	I _{OUT}	0		5	Α	
Resistance	ILIM	40.2	100	162	kΩ	

Change To: (page 4)

 Changed Continuous output current and Change Resistance value					
		MIN	TYP MAX	UNIT	
Continuous output current	lout	0	1.7	A	
Resistance	ILIM	10	45.3	kΩ]

Reason for Change:				
To more accurately reflect device characteristics.				
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):				
Electrical specification performance changes as indicated above.				
Changes to product identification resulting from this PCN:				
None.				
Product Affected:				
TPS2592AADRCR	TPS2592ALDRCT	TPS2592BLDRCR	TPS2592ZADRCT	
TPS2592AADRCT	TPS2592BADRCR	TPS2592BLDRCT		
TPS2592ALDRCR	TPS2592BADRCT	TPS2592ZADRCR		

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com