



STS4DNF60

N-channel 60V - 0.070Ω - 4A - SO-8
STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)}	I _D
STS4DNF60	60V	<0.090Ω	4A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Application

- Switching applications

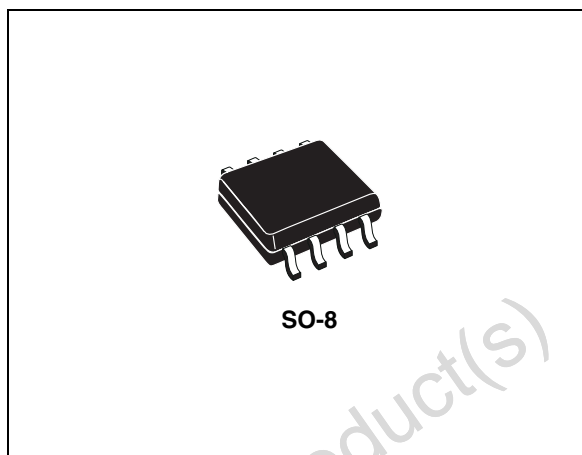


Figure 1. Internal schematic diagram

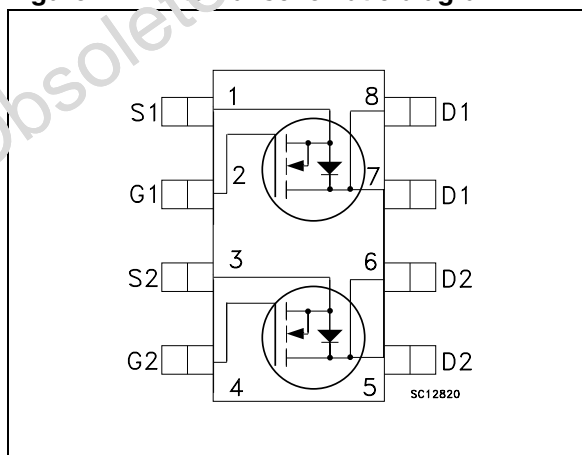


Table 1. Device summary

Order code	Marking	Package	Packaging
STS4DNF60	4DF60	SO-8	Tape & reel

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	2.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	2	W
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $P_{TOT}=1.6\text{W}$ for single operation

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}$	Thermal resistance junction-pcb D.O. ⁽¹⁾	62.5	$^\circ\text{C/W}$

1. When mounted on inch² FR-4 board, 2 Oz Cu, $t \leq 10\text{sec}$, dual operation

2 Electrical characteristics

(T_{case} = 25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250μA, V _{GS} = 0	60			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating, T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20V			± 100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250μA	2		4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 2A		0.070	0.090	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs}	Forward transconductance	V _{DS} = 25V, I _D = 2A		25		S
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		315		pF
C _{oss}	Output capacitance			70		pF
C _{rss}	Reverse transfer capacitance			30		pF
Q _g	Total gate charge	V _{DD} = 48V, I _D = 4A,		10		nC
Q _{gs}	Gate-source charge	V _{GS} = 10V		3.5		nC
Q _{gd}	Gate-drain charge	(see Figure 13)		3.5		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 30V$, $I_D = 2A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 12)		7 18		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 30V$, $I_D = 2A$, $R_G = 4.7\Omega$, $V_{GS} = 10V$ (see Figure 12)		17 6		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4A$, $V_{GS} = 0$			1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 4A$, $di/dt = 100A/\mu s$		45		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20V$, $T_j = 25^\circ C$		68		nC
I_{RRM}	Reverse recovery current	(see Figure 17)		3		A
t_{rr}	Reverse recovery time	$I_{SD} = 4A$, $di/dt = 100A/\mu s$		50		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20V$, $T_j = 150^\circ C$		88		nC
I_{RRM}	Reverse recovery current	(see Figure 17)		3.5		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

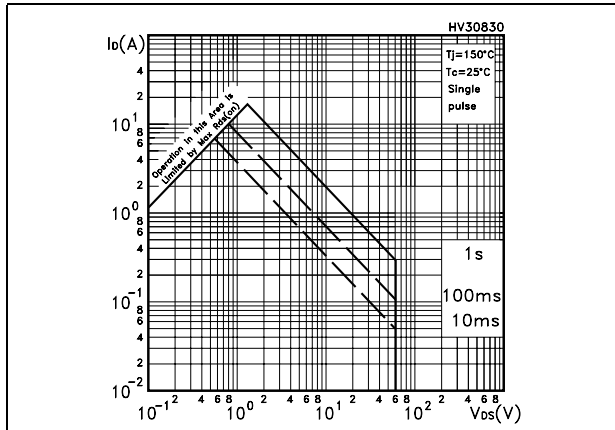


Figure 3. Thermal impedance

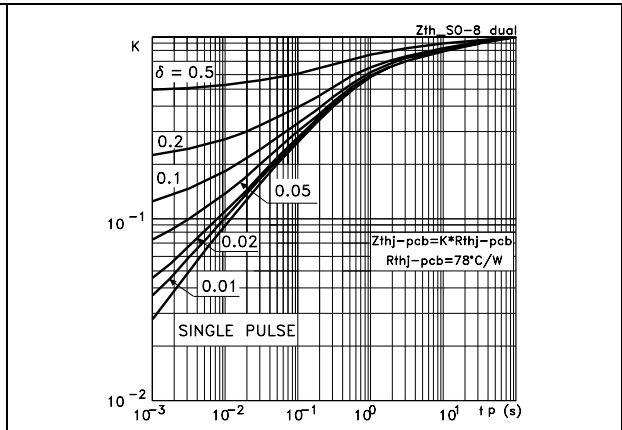


Figure 4. Output characteristics

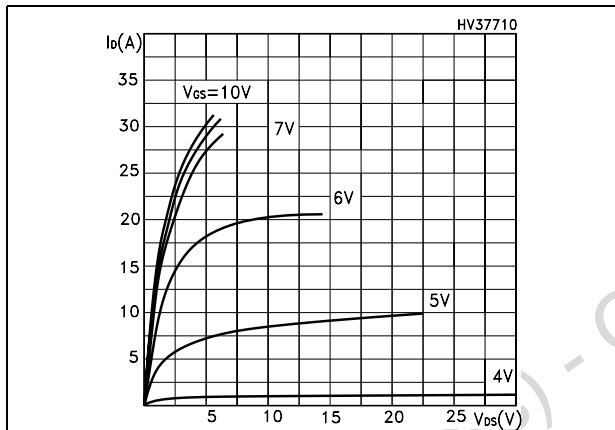


Figure 5. Transfer characteristics

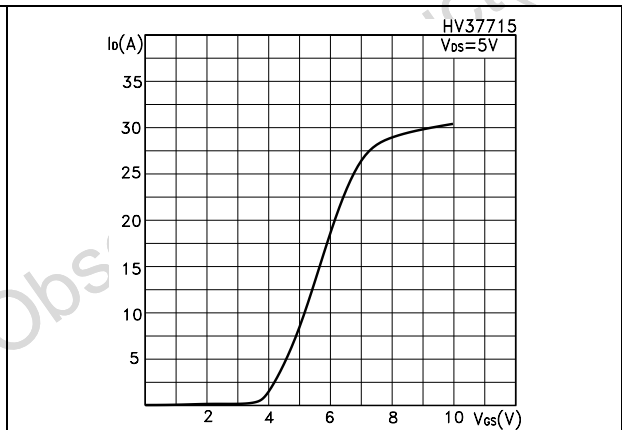


Figure 6. Source-drain diode forward characteristics

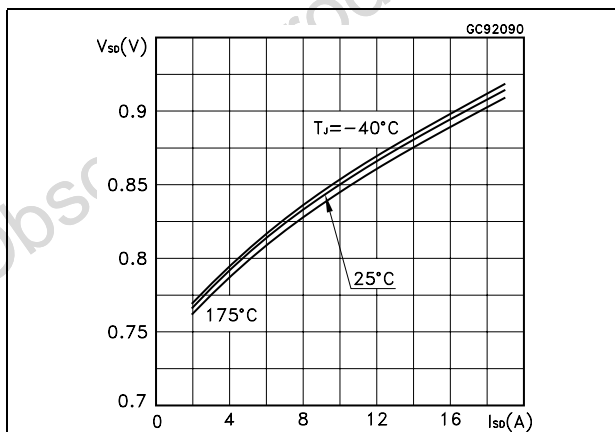


Figure 7. Static drain-source on resistance

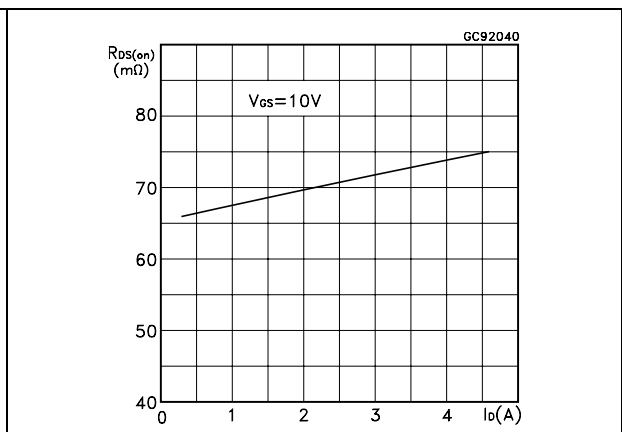


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

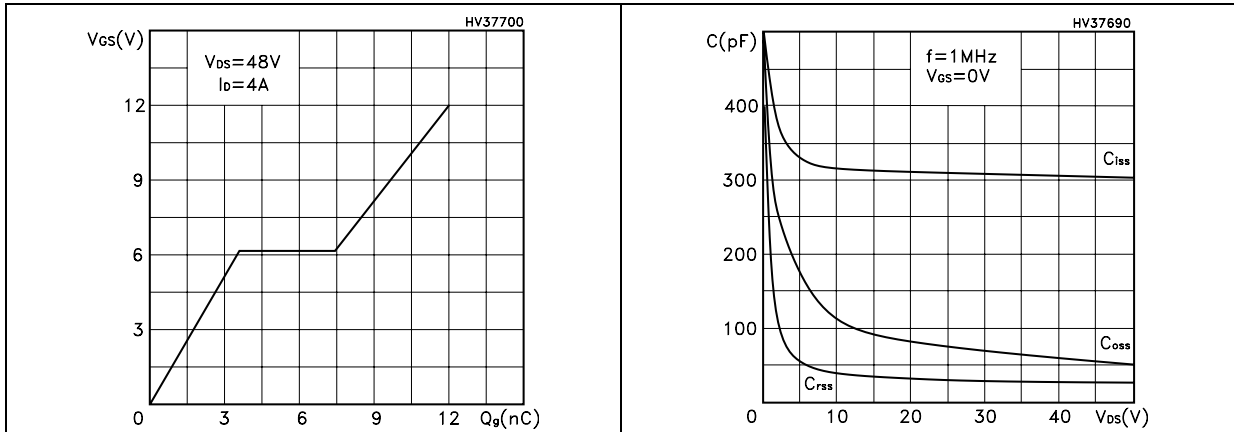
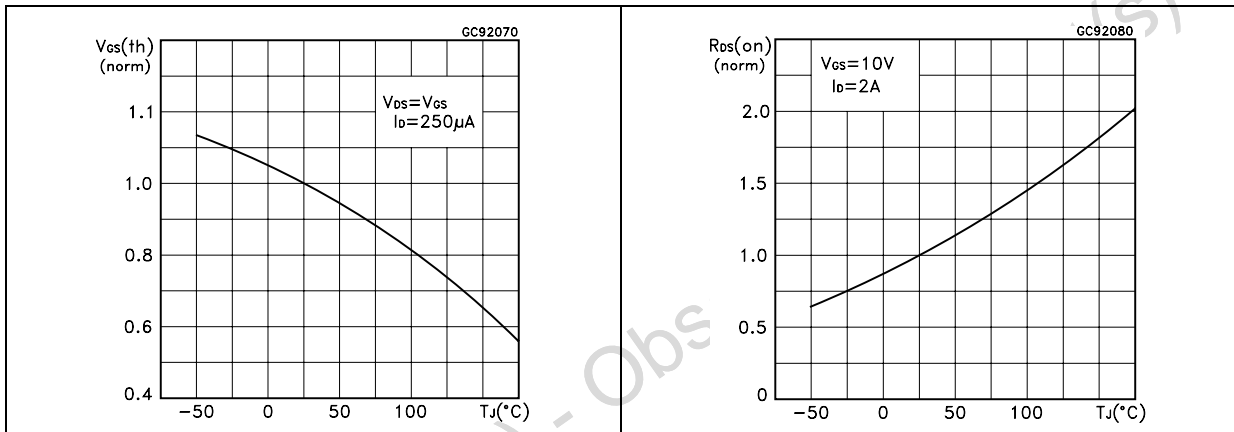


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature



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3 Test circuits

Figure 12. Switching times test circuit for resistive load

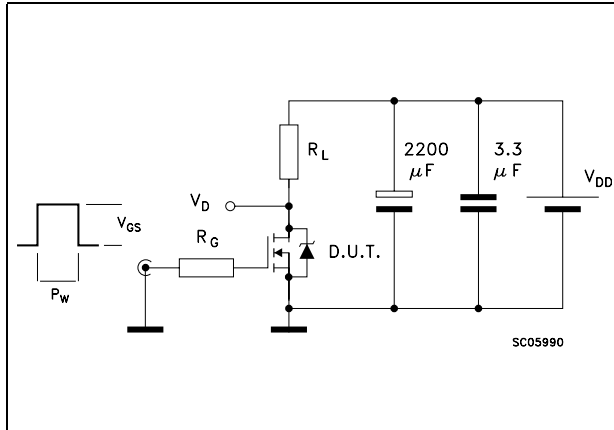


Figure 13. Gate charge test circuit

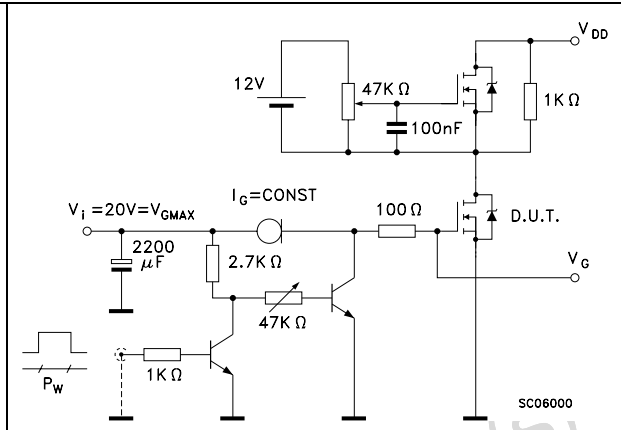


Figure 14. Test circuit for inductive load switching and diode recovery times

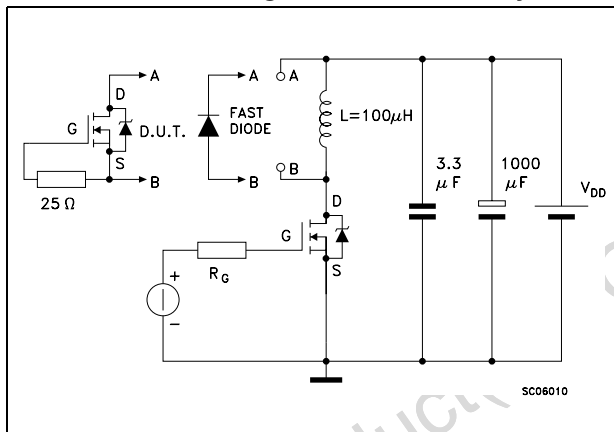


Figure 15. Unclamped Inductive load test circuit

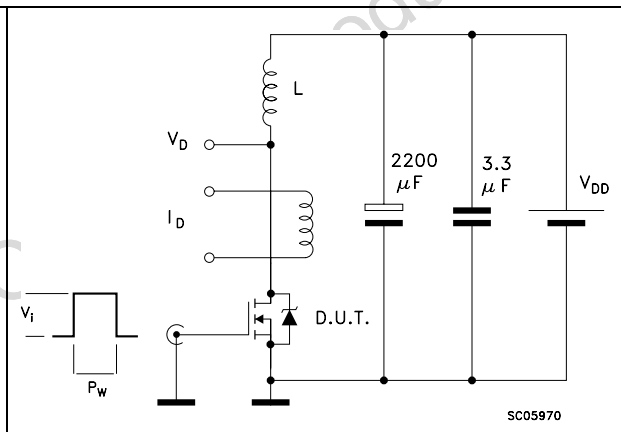


Figure 16. Unclamped inductive waveform

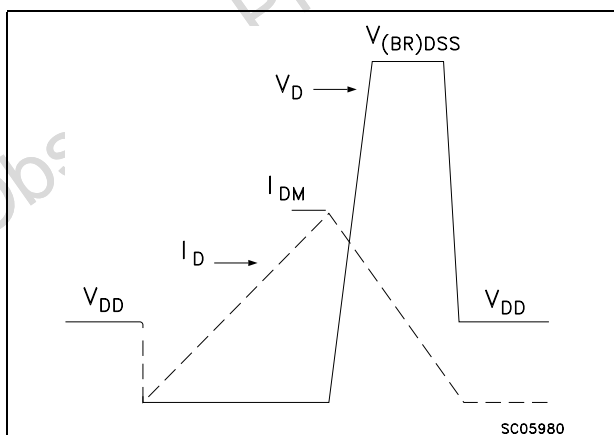
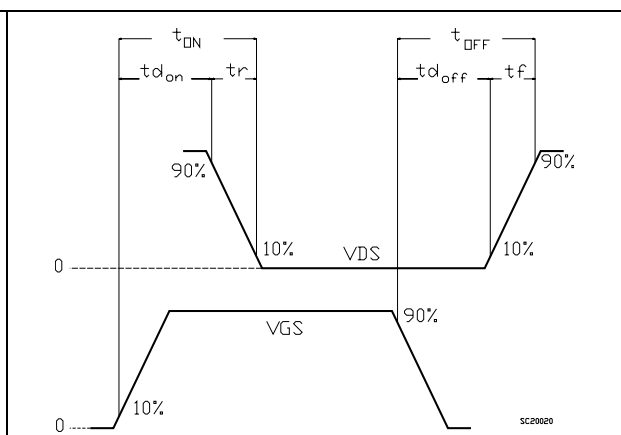


Figure 17. Switching time waveform



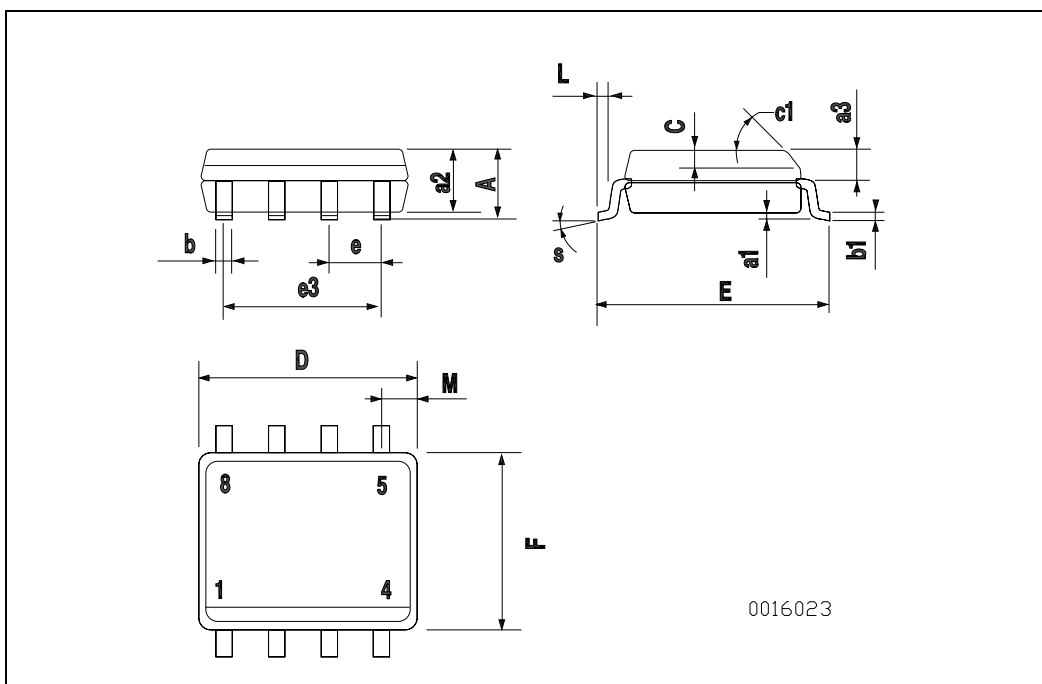
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023

5 Revision history

Table 8. Revision history

Date	Revision	Changes
17-May-2007	1	First release
02-Aug-2007	2	Marking has been updated

Obsolete Product(s) - Obsolete Product(s)

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