PCN Number:		20140627001					_	<b>PCN Date:</b>			06/30/2014		
Title: Wafer Diamet			ter Cl	nang	ge for	Select	DE	F-EP Niche Device	s in	LB	C3S	Proc	ess at DL-LIN
<b>Customer Contact:</b>			<u>PCN</u>	Manager Phon		e:	+1(214)480-603	7	<b>Dept:</b> Qua			ality Services	
*Proposed 1 <sup>st</sup> Ship Da			ite:	09	/30/2	Bo/2014 Estimated Sample Availability:				Date Provided a Sample request			
Change Type:													
	Assen	nbly Site			Assembly Process					Assembly Materials			
	Desig	n			Electrical Specification				Mechanical Specification				
Test Site					Packing/Shipping/Labeling				T	Test Process			
☐ Wafer Bump Site					Wafer Bump Material					٧	Wafer Bump Process		
Wafer Fab Site				Wafer Fab Materials			$\boxtimes$	٧	Vafer	Fab	Process		
					Part number change								
	PCN Details												

## **Description of Change:**

This change notification is to announce a wafer diameter change for select DEF-EP Niche Devices in LBC3S Process at DL-LIN.

Current	New
Site/Process/Wafer Diameter	Site/Process/Wafer Diameter
DL-LIN/LBC3S Process/150mm	DL-LIN/LBC3S Process/200mm

The LBC3S process technology/200mm wafer was previously qualified at DL-LIN and has been running successfully since 2000.

## **Reason for Change:**

Continuity of supply.

# Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

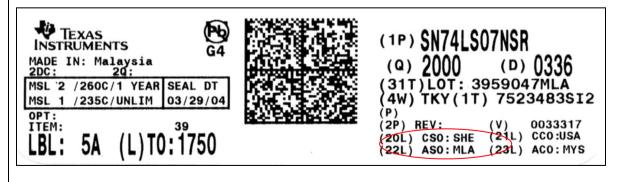
#### Changes to product identification resulting from this PCN:

Note: This is <u>not a fab site change</u>. No change to the Chip Site Location.

#### Current

Chip Site	Chip site code (20L)	Chip country code (21L)				
DL-LIN	DLN	USA				

# Sample Product Shipping Label (not actual product label)



Product Affected:								
TPS79301DBVREP	TPS79333DBVREP	TPS793475DBVREP						

# **Reference Qualification: LBC3s Process at DFAB**

	Qualification Data: (Approved: 2000)								
This qualification has been developed for the validation of this change. The qualification data will validate that the proposed change meets the applicable released									
technical specifications.									
	Qual Vehicle 1: SN104605PN								
Wafer Fab Site:	DFAB		Wafer Diameter: 200	0mm					
Wafer Fab Process:			•-						
Qualification: P	lan	Test Re	sults						
Reliability Test		Conditi	ons		Sample Lot#1	Size/Fai Lot#2	ls Lot#3		
**Life Test		155C (	240hrs)		116/0	116/0	116/0		
**Biased HAST		130C/8	5%RH (96 Hrs)		77/0	77/0	77/0		
**Thermal Shock		-65/+1	50C (1000 Cycles)		77/0	77/0	77/0		
ESD HBM		2.5KV			3/0	3/0	3/0		
Electrical Characteriz	ation	-		Pass	Pass	Pass			
Bond Strength				76/0	76/0	76/0			
Die Shear				5/0	5/0	5/0			
Manufacturability (Wafe	er Fab)	Per site	spec		Approved	-	-		
Manufacturability (Asse	embly)	(per mf	g. Site specification)		Approved	-	-		
**Preconditioning	: Level	3-2350							
Wafan Fala Cita	DEAD	Qua	Vehicle 2: SN75976A						
Wafer Fab Brasses	DFAB LBC3s		Wafer Diameter: 200						
Wafer Fab Process:  Qualification: P		Test Re	culto						
	Iaii			Sample Size/Fails					
Reliability Test		Conditi	ons	Lot#1 Lot#2 Lot#3					
**Life Test		155C (	240hrs)		116/0	116/0	116/0		
ESD HBM		2.5KV		3/0	3/0	3/0			
ESD CDM		1.5KV		3/0	3/0	3/0			
Electrical Characteriz	zation	-			Pass	Pass	Pass		
Latch-Up					5/0	5/0	5/0		
Manufacturability (Wafe	er Fab)	Per site	spec	Approved	-	-			
Manufacturability (Asse	embly)	(per mf	g. Site specification)	Approved	-	-			
**Preconditioning: Level 3-220C									

# **Qualification Results (2000 and 2002)**

### **Automotive Product Qualification Summary**

(As per AEC-Q100 and JEDEC Guidelines)

**Supplier Wafer Fabrication Site:** 

Texas Instruments Dallas fab (DFAB)

Supplier	Code:			Sup	plier Die R	evision:			С			
Supplier	Part Nu	ımber:	SN104605PN	Sup	plier Asser	nbly/Te	st Site:					
Customer Name:					Supplier Package / Pin:				PN/ 80			
Custome	er Part N	lumber:		Pb-	Free Lead F	rame (Y	//N):		Υ			
Device D	escripti	on:		"Gı	reen" Mold	Compo	und (Y/I	N):	Υ			
MSL Rati	ing:		Level1	Op	erating Ten	np Range	e:		-40C to +125C			
Peak Solo	der Ref	low Temp:	220C	Aut	tomotive G	rade Lev	rel (1):		1			
Test	#	Referenc	e Test Conditions		Min Lots (2)	SS / lot (2)	Mi Total		Results Lot/pass/fail	Comments: (N/A =Not Applicable)	Exceptions to AEC -Q100	
			TEST GROUP A – ACCEL	.ERATED	ENVIRON	IMENT:	STRESS	TES	TS (3)			
PC	A1	JESD22-113 J-STD-020	Preconditioning: SMD only; Moisture Preconditionin THB/HAST, AC/UHST, TC, HTSL, and	-	devices	med on a prior to T HST, TC a	тнв/на	ST,				
THB or HAST	A2	JESD22-A10 JESD22-A11	1 Temperature Humidity Bias:		3	77	23:	1	3/231/0			
AC or UHST	A3	JESD22-A10 JESD22-A11			3	77	23:	1	3/231/0	QBS to existing 80PN package data		
TC	A4	JESD22-A10	4 Temperature Cycle: -65°C/+150°C/500 cycles		3	77	23:	1	3/231/0	QBS to existing 80PN		
			Post Temperature Cycle Bond Pull: grams minimum	: 3	1	5	5		1/5/0	package data		
				•		•	•		-		-	
			TEST GROUP B – ACCEL	.ERATED	LIFETIME	SIMUL	ATION	TEST	'S (3)			
HTOL	B1	JESD22-A108	High Temp Operating Life: 125°C/1000 hours 150°C/408 hours		3	-	77	231	3/348/0			
ELFR	B2	AEC-Q100-00	8 Early Life Failure Rate:						. /000/0	QBS to	One lot of	

3

800

2400

1/800/0

Supplier Name:

Texas Instruments Inc.

MAX32431 PWG4DL

One lot of

#### **TEST GROUP C - PACKAGE ASSEMBLY INTEGRITY TESTS (3)**

WBS	C1	AEC-Q100-001	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts min.	30 bonds	Pass		
WBP	C2	Mil-Std-883 Method 2011	Wire Bond Pull: Each bonder used (Cpk > 1.67)	30 bonds	5 parts min.	30 bonds	Pass		
SD	C3	JESD22-B102	Solderability: (>95% coverage) 8 hr steam age (1 hour for Au-plated leads)	1	30	30	1/30/0	QBS to existing 80PN package data	
PD	C4	JESD22-B100 JESD22-B108	Physical Dimensions: (Cpk > 1.67)	3	10	30	3/10/0	QBS to existing 80PN package data	

#### **TEST GROUP E- ELECTRICAL VERIFICATION**

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	Pass		
НВМ	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (2kV - H2 or better)	1	See Test Method			QBS to SN75976A2 DL	
MM	E2	AEC-Q100-003	Electrostatic Discharge, Machine Model: (200V – M3 or better)	1	See Test Method			QBS to SN75976A2 DL	
CDM	E3	AEC-Q100-101	Electrostatic Discharge, Charged Device Model: (750V corner leads, 500V for all other pins)	1	See Test Method		Pass	QBS to SN75976A2 DL	
LU	E4	AEC-Q100-004	Latch-Up:	1	6	6		QBS to SN75976A2 DL	
ED	E5	AEC-Q100-009	Electrical Distributions: (Cpk > 1.67)	1	30	30	Pass		

(1) Grade 0 (or A):  $-40^{\circ}$ C to  $+150^{\circ}$ C ambient operating temperature range

Grade 1 (or Q): -40°C to +125°C ambient operating temperature range

Grade 2 (or T): -40°C to +105°C ambient operating temperature range

Grade 3 (or I):  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ambient operating temperature range

Grade 4 (or C):  $-0^{\circ}$ C to  $+150^{\circ}$ C ambient operating temperature range

(2) These are recommended minimum lot/sample sizes. Lot/sample size may be reduced depending on available data.

(3) Generic data may be used.

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com