

Notification Number:	20150904000	Notification Date:	11/13/2015
Title:	Datasheet update for SN65DSI84		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is updated as seen in the change revision history below:



SN65DSI84

SLLSEC2F – SEPTEMBER 2012 – REVISED AUGUST 2015

www.ti.com

Changes from Revision E (October 2013) to Revision F

Page

• Added Pin Configuration and Functions section, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
• Changed note 2 under Figure 6 for clarification.	12
• Changed ULPS Itemized List, item 3 from "Wait for the PLL_LOCK bit (CSR 0x0A.7) to be set" to "Wait for a minimum of 3 ms."	14
• Changed Initialization Sequence Description for Init seq7 from "Wait for the PLL_LOCK bit to be set (CSR 0x0A.7)" to "Wait for a minimum of 3 ms."	16
• Changed Table 6 Address 0x0A, Bit 7 description from "PLL_LOCK" to "PLL_EN_STAT"	23
• Changed Address 0x18, Bits 3, 2, 1, and 0 Descriptions in Table 8 for clarification.	25
• Changed Item 1 of the Video STOP and Restart sequence from "Clear the PLL_EN bit to 0(CSR 0x0A.7)" to "Clear the PLL_EN bit to 0 (CSR 0x0D.0)"	32

The datasheet number will be changing.

Device Family	Change From:	Change To:
SN65DSI84	SLLSEC2E	SLLSEC2F

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/sn65dsi84>

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this Notification:

None.

Product Affected:

SN65DSI84ZQER

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com