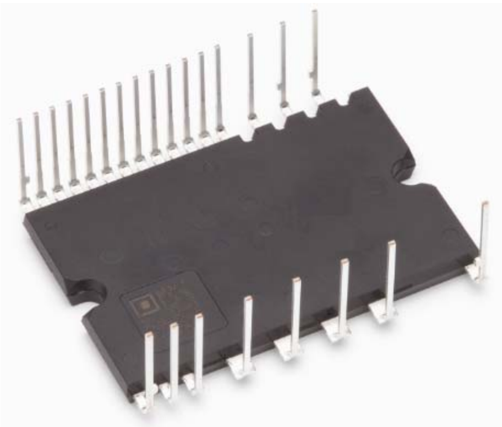
< DIPIPM >

PSM05S93E5-A

TRANSFER MOLDING TYPE
INSULATED TYPE

OUTLINE



MAIN FUNCTION AND RATINGS

- 3 phase DC/AC inverter
- 500V / 5A (MOSFET)
- N-side MOSFET open source
- Built-in bootstrap diodes with current limiting resistor

APPLICATION

- AC 100~240Vrms(DC voltage:400V or below) class low power motor control

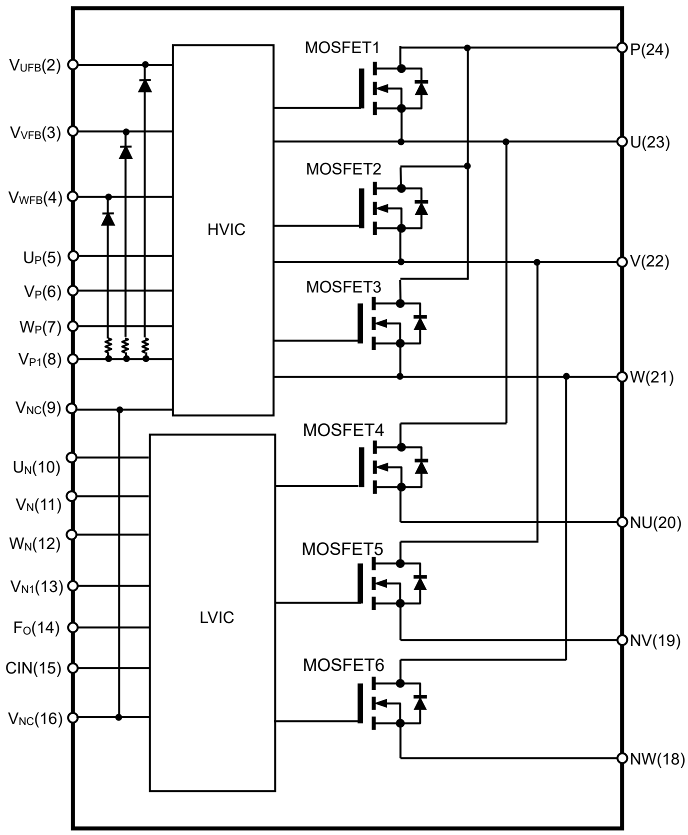
TYPE NAME

PSM05S93E5-A	With over temperature protection

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC), Over temperature protection (OT)
- Fault signaling : Corresponding to SC fault (N-side MOSFET), UV fault (N-side supply) and OT fault
- Input interface : 3, 5V line, Schmitt trigger receiver circuit (High Active)
- UL Recognized : UL1557 File E323585

INTERNAL CIRCUIT



Publication Date : January 2021

MAXIMUM RATINGS (T_{ch} = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{DD}	Supply voltage	Applied between P-NU,NV,NW	400	V
$V_{DD(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	450	V
V_{DSS}	Drain-source voltage		500	V
$\pm I_D$	Each MOSFET drain current	T_C= 25°C (Note 1)	5	A
$\pm I_{DP}$	Each MOSFET drain current (peak)	T_C= 25°C, less than 1ms	10	A
P_D	Drain dissipation	T_C= 25°C, per 1 chip	35.7	W
T_{ch}	Channel temperature	(Note 2)	-20~+150	°C

Note1: Pulse width and period are limited due to channel temperature.
Note2: The maximum junction temperature rating of built-in power chips is 150°C(@Tc≤100°C).However, to ensure safe operation of DIPIPM, the average channel temperature should be limited to Tch(Ave)≤125°C (@Tc≤100°C).

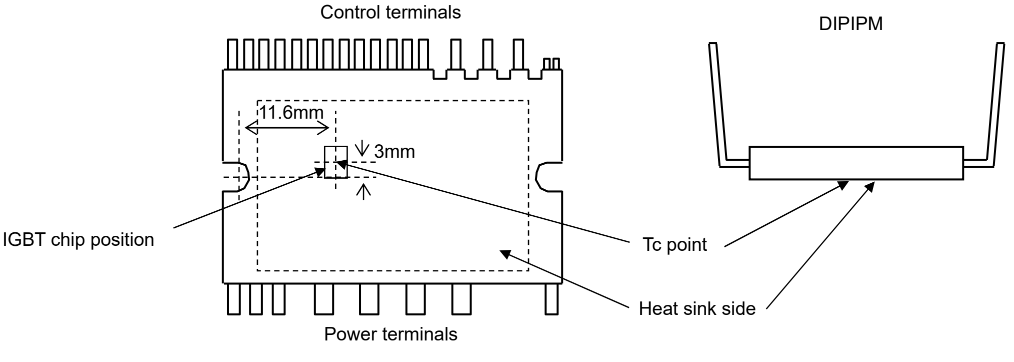
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{DD(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part Tch = 125°C, non-repetitive, less than 2μs	400	V
T_C	Module case operation temperature	Measurement point of Tc is provided in Fig.1	-20~+100	°C
T_{stg}	Storage temperature		-40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}

Fig. 1: T_C MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits Min.	Limits Typ.	Limits Max.	Unit
$R_{th(ch-c)Q}$	Channel to case thermal resistance (Note3)	1/6 module	-	-	2.8	K/W

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•k).

ELECTRICAL CHARACTERISTICS (T_{ch} = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits Min.	Typ.	Max.	Unit
$V_{DS(on)}$	Drain-source on-state resistance	V_D=V_{DB} = 15V, V_{IN}= 5V, I_D= 5A	T_{ch}= 25°C	-	0.60	0.80	Ω
			T_{ch}= 125°C	-	1.30	1.70	
V_{SD}	Source-drain voltage drop	V_{IN}= 0V, -I_D= 5A		-	0.90	1.30	V
t_{on}	Switching times	V_{DD}= 300V, V_D= V_{DB}= 15V I_D= 5A, Tch= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		0.65	1.15	1.65	μs
$t_{C(on)}$				-	0.35	0.55	μs
t_{off}				-	1.00	1.50	μs
$t_{C(off)}$				-	0.10	0.20	μs
t_{rr}				-	0.25	-	μs
I_{DSS}	Drain-source cut-off current	V_{DS}=V_{DSS}	T_{ch}= 25°C	-	-	1	mA
			T_{ch}= 125°C	-	-	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits Min.	Typ.	Max.	Unit
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	2.80	mA
			V_D=15V, V_{IN}=5V	-	-	2.80	
I_{DB}		Each part of V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.10	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 4)		0.43	0.48	0.53	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	Tch ≤125°C	Trip level	7.0	10.0	12.0	V
UV_{DBr}			Reset level	7.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
OT_t	Over temperature protection (OT) (Note5)	V_D = 15V Detect LVIC temperature	Trip level	100	120	140	°C
OT_{rh}			Hysteresis of trip-reset	-	10	-	°C
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 6)		20	-	-	μs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	2.10	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.30	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.65	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor (Note 7)		1.1	1.7	2.3	V
R	Built-in limiting resistance	Included in bootstrap Di		80	100	120	Ω

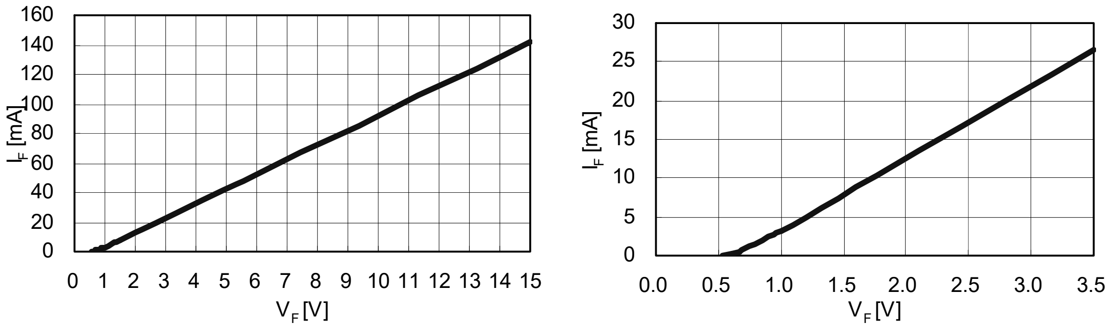
Note 4 : SC protection works for N-side only. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and Fo outputs. In that case if the heat sink dropped off or fixed loosely, don't reuse that DIPIPM. (There is a possibility that channel temperature of power chips exceeded maximum Tch(150°C).

6 : Fault signal Fo outputs when SC, UV or OT protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20μs), but at UV or OT failure, Fo outputs continuously until recovering from UV or OT state. (But minimum Fo pulse width is 20μs.)

7 : The characteristics of bootstrap Di is described in Fig.2.

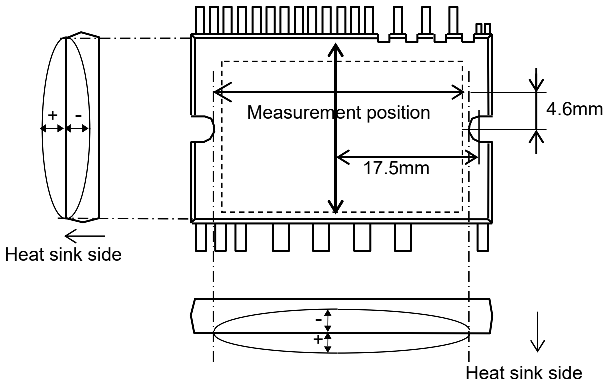
Fig. 2 Characteristics of bootstrap Di V_F-I_F curve (@Ta=25°C) including voltage drop by limiting resistor (Right chart is enlarged chart.)



MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw : M3 (Note 8)	Recommended 0.69N·m	0.59	0.69	0.78	N·m
Terminal pulling strength	Control terminal: Load 4.9N Power terminal: Load 9.8N	JEITA-ED-4701	10	-	-	s
Terminal bending strength	Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend	JEITA-ED-4701	2	-	-	times
Weight			-	8.5	-	g
Heat-sink flatness	(Note 9)		-50	-	100	μm

Note 8: Plain washers (ISO 7089~7094) are recommended.
Note 9: Measurement point of heat sink flatness



RECOMMENDED OPERATION CONDITIONS

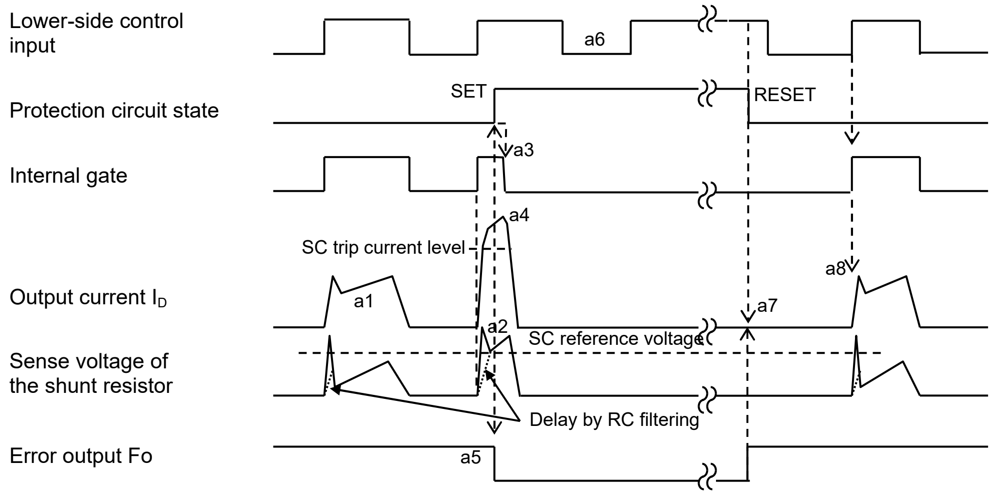
Symbol	Parameter	Condition		Limits Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	Applied between P-NU, NV, NW		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal		1.0	-	-	μs
f_{PWM}	PWM input frequency	$T_C \le 100°C$, $Tch \le 125°C$		-	-	20	kHz
I_O	Allowable r.m.s. current	V_{DD} = 300V, V_D = 15V, P.F = 0.8, Sinusoidal PWM $T_C \le 100°C$, $Tch \le 125°C$ (Note10)	f_{PWM}= 5kHz	-	-	2.5	Arms
			f_{PWM}= 15kHz	-	-	2.0	
PWIN(on)	Minimum input pulse width	(Note 11)		0.7	-	-	μs
PWIN(off)				0.7	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		-5.0	-	+5.0	V
Tch	Channel temperature			-20	-	+125	°C

Note 10: Allowable r.m.s. current depends on the actual application conditions.
11: DIPIPM might not make response if the input signal pulse width is less than PWIN(on), PWIN(off).

Fig. 3 Timing Charts of The DIPIPM Protective Functions

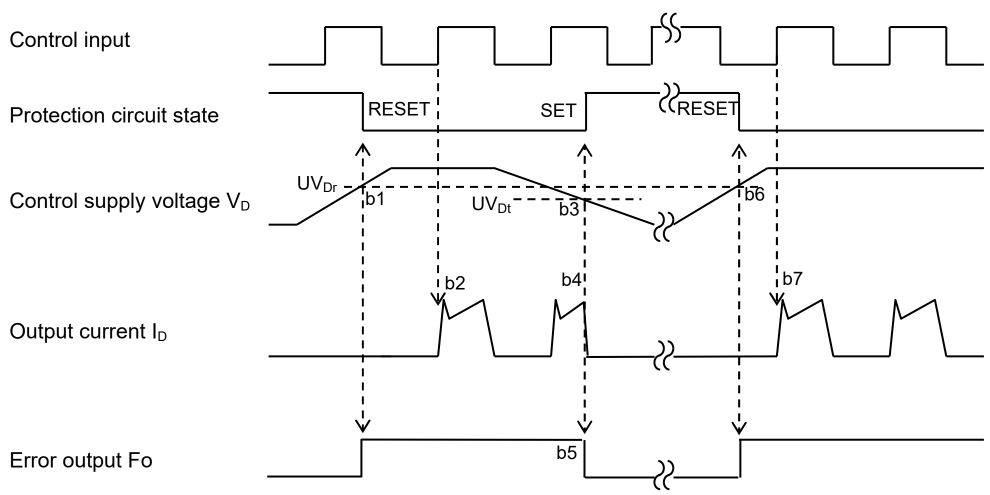
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: MOSFET ON and outputs current.
a2. Short circuit current detection (SC trigger)
(It is recommended to set RC time constant 1.5~2.0μs so that MOSFET shut down within 2.0μs when SC.)
a3. All N-side MOSFET's gates are hard interrupted.
a4. All N-side MOSFETs turn OFF.
a5. F_O outputs for t_{Fo}=minimum 20μs.
a6. Input = "L": MOSFET OFF
a7. Fo finishes output, but MOSFETs don't turn on until inputting next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
a8. Normal operation: MOSFET ON and outputs current.



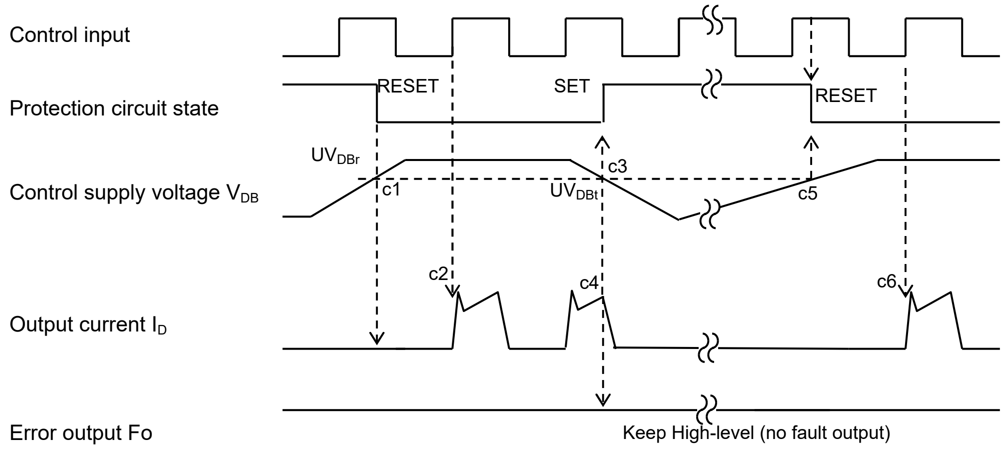
[B] Under-Voltage Protection (N-side, UV_D)

b1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
b2. Normal operation: MOSFET ON and outputs current.
b3. V_D level drops to under voltage trip level. (UV_{Dt}).
b4. All N-side MOSFETs turn OFF in spite of control input condition.
b5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.
b6. V_D level reaches UV_{Dr}.
b7. Normal operation: MOSFET ON and outputs current.



[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, MOSFET turns on by next ON signal (L→H).
c2. Normal operation: MOSFET ON and outputs current.
c3. V_{DB} level drops to under voltage trip level (UV_{DBt}).
c4. MOSFET of the correspond phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
c5. V_{DB} level reaches UV_{DBr}.
c6. Normal operation: MOSFET ON and outputs current.



[D] Over Temperature Protection (N-side, Detecting LVIC temperature)

d1. Normal operation: MOSFET ON and outputs current.
d2. LVIC temperature exceeds over temperature trip level(OT_t).
d3. All N-side MOSFETs turn OFF in spite of control input condition.
d4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
d5. LVIC temperature drops to over temperature reset level.
d6. Normal operation: MOSFET turns on by next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)

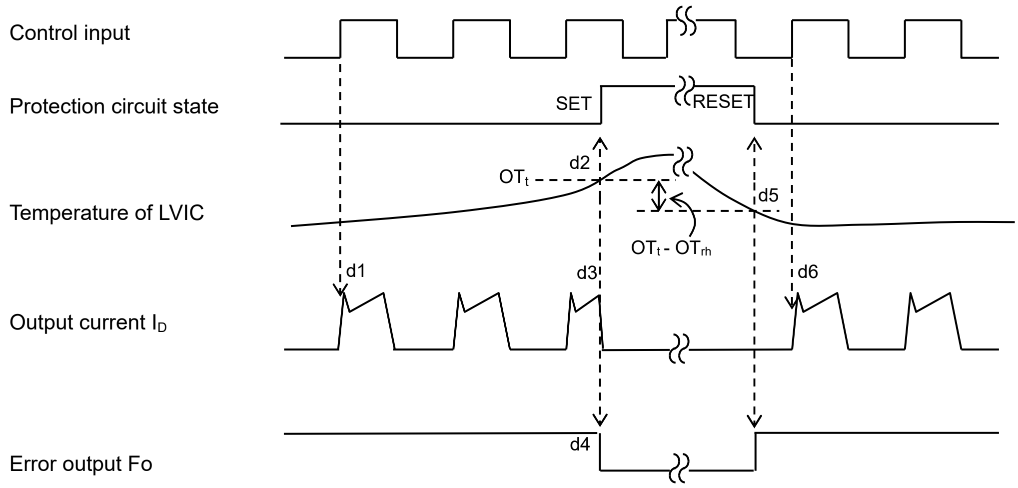
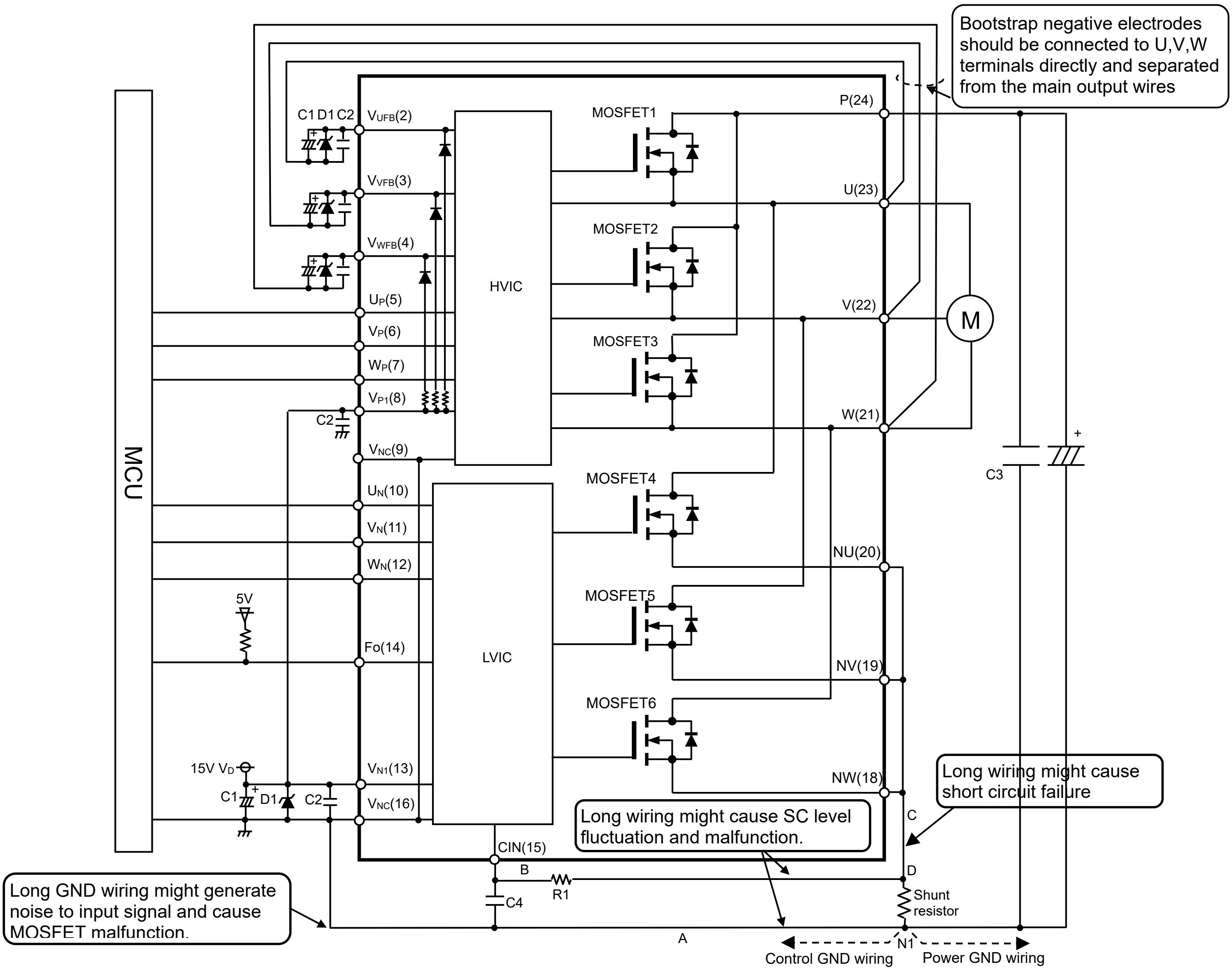
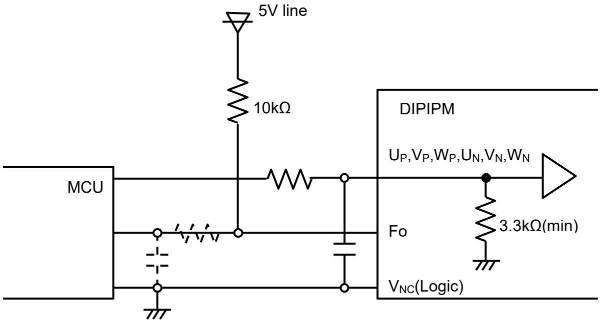


Fig. 4 Example of Application Circuit



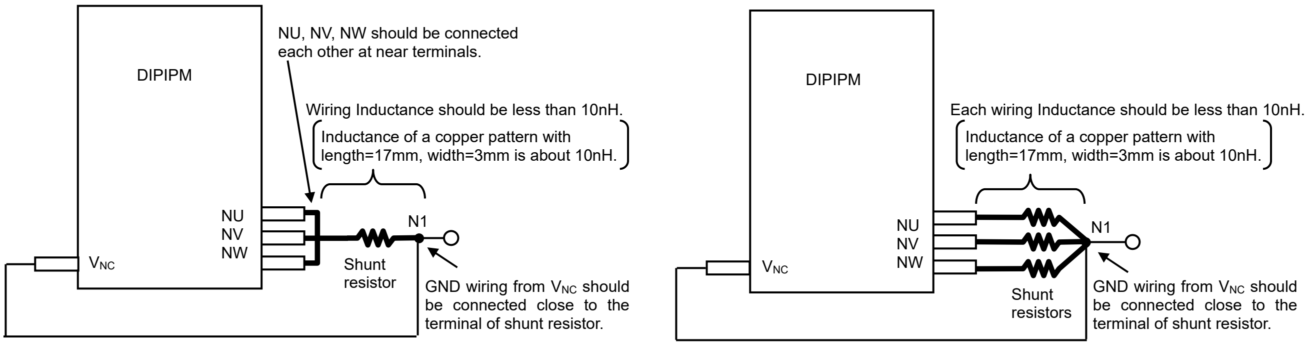
(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.
(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
(8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.
(9) Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)
(10) Thanks to built-in HVIC, direct coupling to MCU without any opto-coupler or transformer isolation is possible.
(11) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.
(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.
(13) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase MOSFET or other DIPIPM.

Fig. 5 MCU I/O Interface Circuit



Note)
Design for input RC filter depends on PWM control scheme used in the application and wiring impedance of the printed circuit board.
DIPIPM input signal interface integrates a minimum 3.3kΩ pull-down resistor. Therefore, when inserting RC filter, it is necessary to satisfy turn-on threshold voltage requirement.
Fo output is open drain type. It should be pulled up to control power supply (e.g. 5V, 15V) with a resistor that makes Fo sink current I_{Fo} 1mA or less. In the case of pulled up to 5V supply, 10kΩ（5kΩ or more）is recommended.

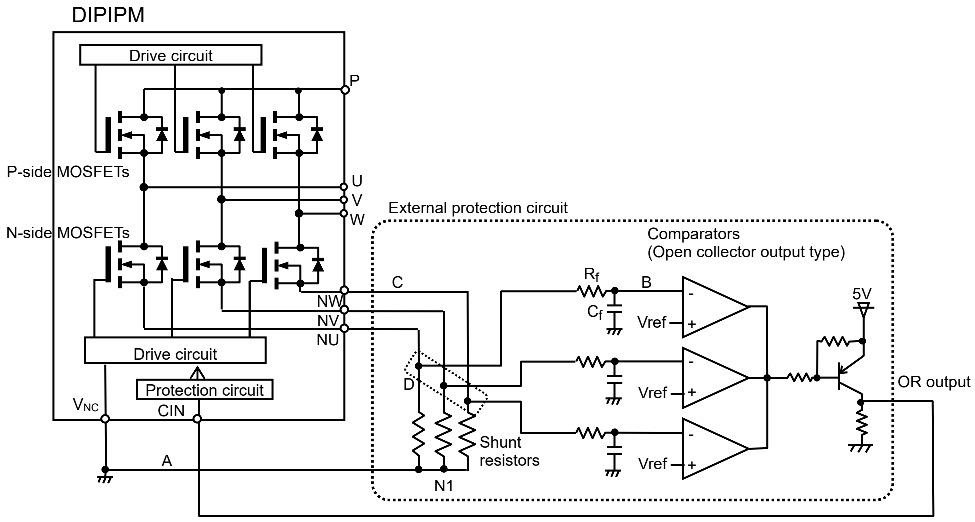
Fig. 6 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Fig. 7 Pattern Wiring Around the Shunt Resistor (for the case of open source)

When DIPIPM is operated with three shunt resistors, voltage of each shunt resistor cannot be input to CIN terminal directly. In that case, it is necessary to use the external protection circuit as below.

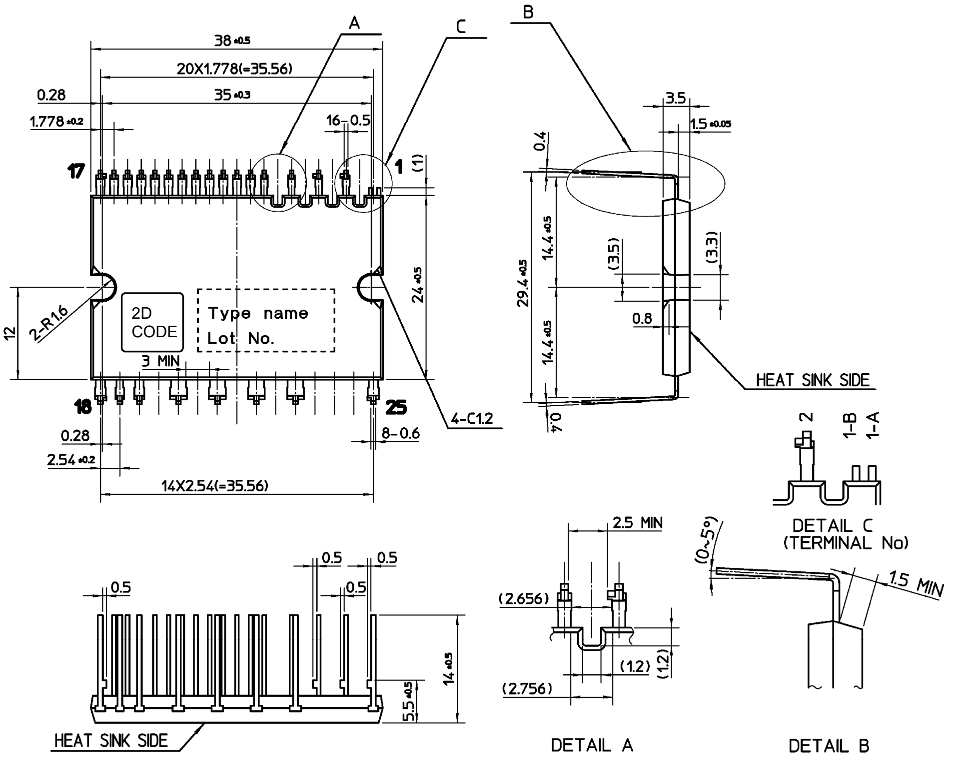


(1) It is necessary to set the time constant R_fC_f of external comparator input so that MOSFET stops within 2μs when short circuit occurs.
SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) It is recommended for the threshold voltage Vref to set to the same rating of short circuit trip level (Vsc(ref): typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified value (=1.7 times of rating current).
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be close to the terminal of shunt resistor.
(6) OR output high level when protection works should be over 0.53V (=maximum Vsc(ref) rating).

Fig. 8 Package Outlines

Long terminal type (PSM05S93E5-A)

Dimensions in mm



TERMINAL CODE

1-A	NC(V_{NC})
1-B	NC(V_{P1})
2	V_{UFB}
3	V_{VFB}
4	V_{WFB}
5	U_P
6	V_P
7	W_P
8	V_{P1}
9	V_{NC} *1
10	U_N
11	V_N
12	W_N
13	V_{N1}
14	Fo
15	CIN
16	V_{NC} *1
17	NC
18	NW
19	NV
20	NU
21	W
22	V
23	U
24	P
25	NC

1) 9 & 16 pins (V_{NC}) are connected inside DIPIPM, please connect either one to the control power supply GND outside and leave another one open.

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