PCN Number:	20180615000.2**A**	**PCN Date:**	Oct 15, 2018
Title:	TLV70025Q1, TLV70033Q Design Change and Datasheet Updates		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	Dec 21, 2018	**Estimated Sample Availability:**	Date provided at sample request.

Change Type:					
☐	Assembly Site	☐	Assembly Process	☐	Assembly Materials
☐	Assembly Site	☒	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

Revision A is to communicate changes in the minimum and maximum current limit sense resistor values that were in error or not communicated on the original PCN notification. The new datasheet revision is highlighted and **bolded** below.
There is no change proposed 1st ship date of December 21, 2018.

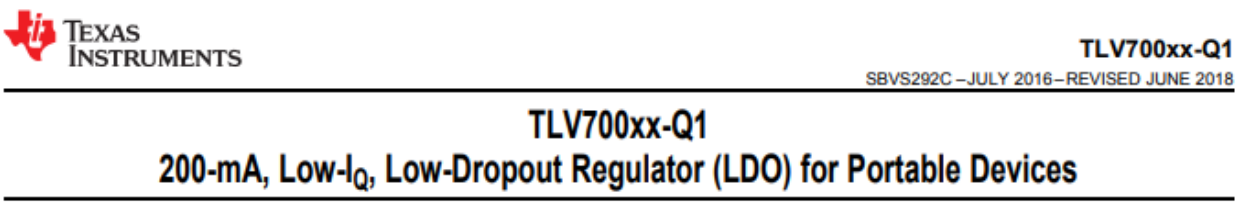
This notification is to inform of a design change to the TLV70025QDDCRQ1 and TLV70033QDDCRQ1 devices. Affected devices are listed in the Product Affected section of this document. The design changes are summarized as follows:

1. Metal 3 change to eliminate cold temp bandgap startup failures.
2. The feedback resistor divider was re-wired to use the existing OTP (One Time Programming EPROM cell) control instead of metal mask programming.
3. ~~The current limit sense resistor value was changed to move the minimum current limit from 220mA to 330mA to provide more margin in manufacturing.~~ **The minimum current limit will remain at 220mA.**
4. A spare bond pad and its associated ESD cell were removed.
5. **The current limit sense resistor value was changed to move the maximum current limit from 550 to 860mA.**

The datasheet numbers will also be changing:

Devices	**Current** Datasheet Number	**New Datasheet Number**
TLV70025QDDCRQ1, TLV70033QDDCRQ1	SLVSA61H	SBVS292C

The product datasheet(s) is updated as seen in the change revision history below:


TEXAS INSTRUMENTS

TLV700xx-Q1

SBVS292C – JULY 2016 – REVISED JUNE 2018

TLV700xx-Q1

200-mA, Low-I_Q, Low-Dropout Regulator (LDO) for Portable Devices

4 Revision History

Changes from Revision B (October 2016) to Revision C — **Page**

- Added DCK (SC70) package to document; note that TLV70025-Q1 and TLV70033-Q1 were previously listed in SLVSA61 1
- Changed *Fixed Output Voltages* bullet to *Fixed Output Voltage Combination* in *Features* section 1
- Changed last paragraph of Description section to include the SC70 package 1
- Added SC70 row to *Device Information* table 1
- Added DCK package to *Pin Configuration and Functions* section 3
- Added T_J parameter to *Absolute Maximum Ratings* table 3
- Changed T_J parameter to T_A in *Recommended Operating Conditions* table and changed *junction* to *ambient* in parameter name 4
- Added *TLV70033-Q1 PSRR Ratio* figure 8

These changes may be reviewed at the datasheet links provided:
http://www.ti.com/lit/ds/symlink/tlv700xx-q1.pdf

Reason for Change:

Fix false bandgap cold temp failures.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Product Affected:

TLV70025QDDCRQ1	TLV70033QDDCRQ1

Automotive New Product Qualification Summary

(As per AEC-Q100 and JEDEC Guidelines)

TLV70025QDDCRQ1 and TLV70033QDDCRQ1 using LTLV703AINZ (Automotive)
Approved 15-May-2018

Product Attributes

Attributes	Qual Device: TLV70025QDDCRQ1	Qual Device: TLV70033QDDCRQ1	QBS Product Reference: TLV70033QDDCRQ1	QBS Product Reference: TLV70225QDSERQ1	QBS Process Reference: SN0406082PW-B1	QBS Package Reference: TPS3700QDDCRQ1	QBS Package Reference: TPS3702EX33QDDCRQ1
Operating Temp Range	-40 to +125 deg C	-40 to +125 C	-40 to +125 C	-40 to +125 C	-40 to +125 C	-40 to +125 C	-40 to +125 C
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Product Function	Power Management	Power Management	Power Management	Power Management	Power Management	Power Management	Power Management
Wafer Fab Supplier	MIHO 8	MIHO8	MIHO8	MIHO-8	MIHO8	RFAB	RFAB
Die Revision	A	A	A	A	BT	A	B
Assembly Site	NS2	NS2	NSE-THAILAND	NSE (OTAC)	YAI	NS2 (OTAC2)	NS2
Package Type	TSOT-23	TSOT-23	TSOT-23	WSON	TSSOP	SOT	SOT
Package Designator	DDC	DDC	DDC	DSE	PW	DDC	DDC
Ball/Lead Count	5	5	5	6	16	6	6

- QBS: Qual By Similarity
- Qual Devices qualified at LEVEL2-260CG: TLV70033QDDCRQ1, TLV70025QDDCRQ1

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name / Condition	Duration	Qual Device: TLV70025QDDCRQ1	Qual Device: TLV70033QDDCRQ1	QBS Product Reference: TLV70033QDDCRQ1	QBS Product Reference: TLV70225QDSERQ1	QBS Process Reference: SN0406082PW-B1	QBS Package Reference: TPS3700QDDCRQ1	QBS Package Reference: TPS3702EX33QDDCRQ1
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning	Level 1-260C	-	-	-	3/844/0	-	-	-
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Automotive Preconditioning	Level 2-260C	-	-	1/250/0	-	-	1/77/0	3/720/0
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 130C/85%RH	96 Hours	-	-	1/77/0	3/231/0	3/231/0	1/77/0	9/231/0
AC	A3	JEDEC JESD22-A102	3	77	Autoclave 121C	96 Hours	-	-	1/77/0	3/231/1 (Note1)	3/230/0	1/77/0	3/231/0
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	-	-	-	3/231/0	3/231/0	1/77/0	3/231/0
TC-BP	A4	MIL-STD883 Method 2011	1	60	Post Temp Cycle Bond Pull	Wires	-	-	-	1/30/0	1/5/0	1/10/0	1/5/0
PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	N/A	-	-	-	-	-
PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle, -40/125C	1000 Cycles	-	-	-	1/45/0	1/45/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp. Storage Bake, 150C	2000 Hours	-	-	-	-	3/224/0	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp. Storage Bake, 175C	500 Hours	-	-	1/52/0	1/45/0	-	1/52/0	2/100/0
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	1000/HRS	-	-	-	-	-	-	3/231/0
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 140C	480 Hours	-	-	-	-	3/229/0 (Note 2)	-	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 150C	408 Hours	-	-	-	3/231/0	-	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 140C	48 Hours	-	-	-	-	3/2409/0	-	-
EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A	N/A	-	-	-	-	-
WBS	C1	AEC Q100-001	1	30	Bond Shear (Cpk>1.67)	Wires	-	-	-	1/30/0	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	-	-	-	1/30/0	-	-	2/60/0
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability >95% Lead Coverage	Pb and Pb-Free	-	-	-	-	-	-	2/60/0
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	--	-	-	-	-	-	-	3/90/0
SBS	C5	AEC Q100-010	3	50	Solder Ball Shear (Cpk>1.67)	Post HTSL/Bump	N/A for this package	N/A for this package	-	-	-	-	-
LI	C6	JEDEC JESD22-B105	1	50	Lead Integrity	Leads	-	-	-	-	-	-	-
EM	D1	JESD61	-	-	Electromigration	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	-	-	-	-	-
TDDB	D2	JESD35	-	-	Time Dependant Dielectric Breakdown	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	-	-	-	-	-
HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	-	-	-	-	-
NBTI	D4	-	-	-	Negative Bias Temperature Instability	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	-	-	-	-	-
SM	D5	-	-	-	Stress Migration	--	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	-	-	-	-	-
HBM	E2	AEC Q100-002	1	3	ESD - HBM	3000 V	1/3/0	-	-	-	-	-	1/3/0
CDM	E3	AEC Q100-011	1	3	ESD - CDM	1500 V	1/3/0	-	-	-	1/3/0	-	-
LU	E4	AEC Q100-004	1	6	Latch-up	(Per AEC-Q100-004)	1/6/0	-	-	1/6/0	1/6/0	1/6/0	1/6/0
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, Hot, & Cold	1/30/0	1/30/0	-	3/90/0	-	2/60/0	3/90/0
ED	E5	AEC Q100-009	3	30	Electrical Characterization	Per Datasheet Parameters	-	-	-	-	3/90/0	-	-

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I) : -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST
-
Note 1: 1 unit discounted for EOS per QTS431043-1.
Note 2: 2 units discounted for lead damage during e-test.
-

Green/Pb-free Status:
Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com