

Vishay Siliconix

ROF

COMPLIANT

N-Channel 100 V (D-S) 175 °C MOSFET

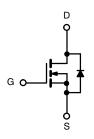
PRODUCT SUMMARY					
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)			
100	0.0165 at V _{GS} = 10 V	60			
	0.0190 at V _{GS} = 6 V	56			

FEATURES

- TrenchFET® Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package •
- PWM Optimized for Fast Switching •
- 100 % R_a and UIS Tested
- Compliant to RoHS Directive 2002/95/EC •

APPLICATIONS

 Isolated DC/DC converters - Primary-Side Switch



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	100	V		
Gate-Source Voltage	V _{GS}	± 20	- V		
Continuous Drain Current (T ₁ = 175 °C)	T _C = 25 °C	I	60 ^a		
	T _C = 125 °C	D'D	34 ^a	A	
Pulsed Drain Current	I _{DM}	100			
Avalanche Current		I _{AS}	40	1	
Single Pulse Avalanche Energy ^b	L = 0.1 mH	E _{AS}	80	mJ	
	T _C = 25 °C	Р	150 ^c	14/	
Maximum Power Dissipation ^b	T _A = 25 °C ^d	– P _D –	3.75	W	
Operating Junction and Storage Temperature Ra	nge	T _J , T _{stq}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Limit	Unit		
Junction-to-Ambient	PCB Mount (TO-263) ^d	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)		R _{thJC}	1.0	0/00		

Notes:

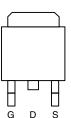
a. Package limited.

b. Duty cycle \leq 1 %.

c. See SOA curve for voltage derating.

d. When mounted on 1" square PCB (FR-4 material).

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TO-263

Ordering Information: SUM60N10-17-E3 (Lead (Pb)-free)

Top View

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{DS} = 0 V, I_{D} = 250 \mu A$	100			V	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2		4		
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			1	50 μA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$			50		
		$V_{DS} = 80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	100			Α	
		V _{GS} = 10 V, I _D = 30 A		0.013	0.0165		
	P	$V_{GS} = 6 V, I_D = 20 A$		0.015	0.019		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V_{GS} = 10 V, I_{D} = 30 A, T_{J} = 125 °C			0.031	Ω	
		V _{GS} = 10 V, I _D = 30 A, T _J = 175 °C			0.041		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	25			S	
Dynamic ^b	4		4	4	• •		
Input Capacitance	C _{iss}			4300		pF	
Output Capacitance	C _{oss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		450			
Reverse Transfer Capacitance	C _{rss}			175			
Total Gate Charge ^c	Qg			65	100	nC	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 60 \text{ A}$		25			
Gate-Drain Charge ^c	Q _{gd}			19			
Gate Resistance	R _g	f = 1 MHz	0.3	1.5	3	Ω	
Turn-On Delay Time ^c	t _{d(on)}			15			
Rise Time ^c	t _r	V_{DD} = 50 V, R_L = 1.5 Ω		12	20	ns	
Turn-Off Delay Time ^c	t _{d(off)}	$\text{I}_\text{D}{\cong}60$ A, V_GEN = 10 V, R_G = 2.5 Ω		30	45		
Fall Time ^c	t _f			10	15		
Source-Drain Diode Ratings and Cha	aracteristics (T _C = 25 °C) ^b			I		
Continuous Current	I _S				60	٨	
Pulsed Current	I _{SM}				100	A	
Forward Voltage ^a	V _{SD}	$I_{F} = 30 \text{ A}, V_{GS} = 0 \text{ V}$		1.0	1.5	V	
Reverse Recovery Time	t _{rr}			125	200	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 50 A, dl/dt = 100 A/μs		8	12	Α	
Reverse Recovery Charge	Q _{rr}			0.5	1.2	μC	

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



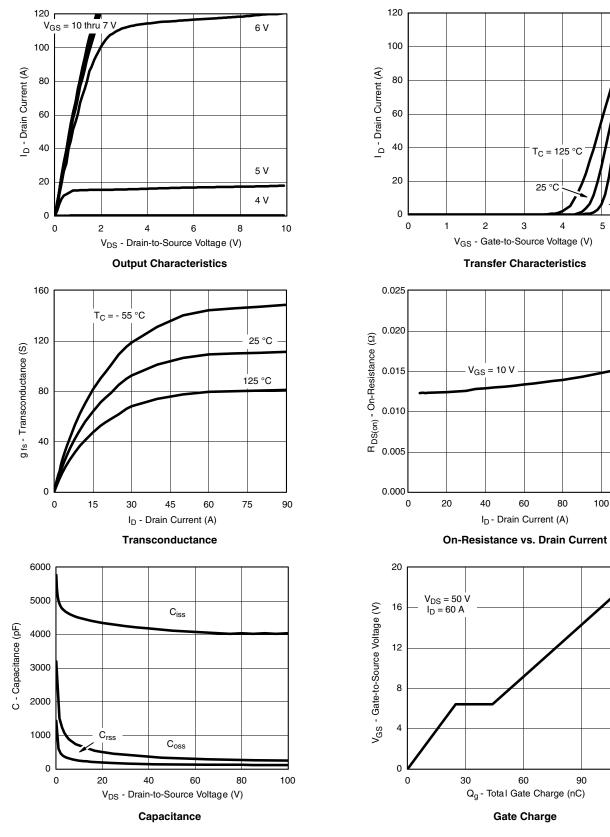
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55 °C

6

120





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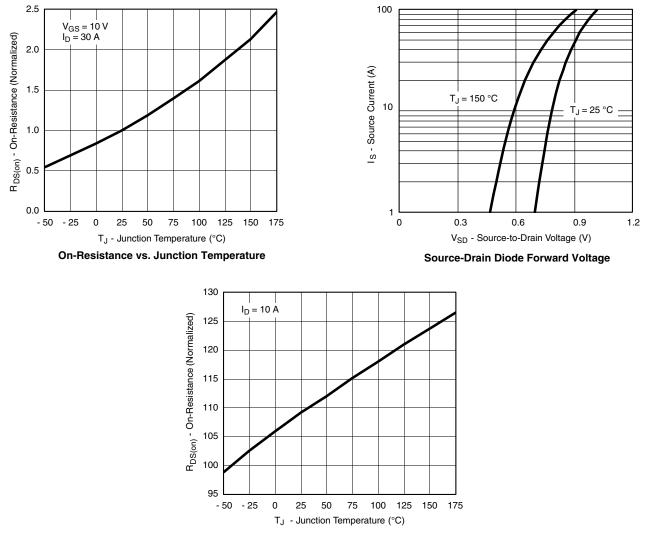
120

3

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

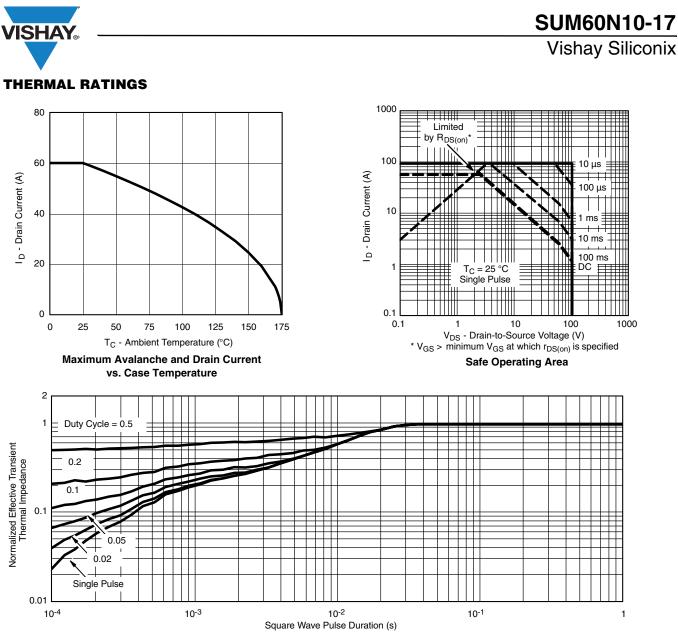


On-Resistance vs. Junction Temperature

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Normalized Thermal Transient Impedance, Junction-to-Case

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5



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TO-263 (D²PAK): 3-LEAD









DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
А		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
D4		0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100 BSC		2.54 BSC		
	К	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
	L3	0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB.
 - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

Revison: 30-Sep-13



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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