LM5127-Q1 2.2-MHz Wide VIN Automotive Front-stage Multi-rail DC/DC

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Suited for various architectures and scalable
  - Triple-output synchronous controllers
  - Flexible topology
    - CH1: boost / buck topology
    - CH2, CH3: two single phase bucks / dual-phase interleaved buck topology
  - Enable pin and PGOOD indicator per channel
  - Optional low I_Q battery monitor
- Wide operating range for automotive applications
  - 3.8-V to 42-V input operating range
  - Minimum boost input 0.8 V when BIAS ≥ 3.8 V
  - Boost output: adjustable up to 42 V
  - Buck output: fixed 3.3 V, 5 V, or adj. 0.8 - 42 V
  - Bypass operation when V_{SUPPLY}>V_{LOAD} (boost)
  - LDO operation when V_{SUPPLY} ≈ V_{LOAD} (buck)
- Minimized battery drain
  - Shutdown current ≤ 2.8 µA
  - Automatic transition to low-I_Q sleep mode
  - Battery drain in sleep
    - I_Q≤ 14 µA when 3.3-V buck on
    - I_Q≤ 22 µA when 3.3-V and 5-V bucks on
    - I_Q≤ 32 µA when 3.3-V, 5-V bucks on and boost in bypass
  - High efficiency using strong 5-V drivers
  - Dual input VCC and VDD regulators
- Small and cost-effective solution
  - Maximum switching frequency 2.2 MHz
  - Internal boot diode (boost)
  - Constant peak current limit
  - Supports DCR inductor current sensing
  - QFN-48 with wettable flanks
- Avoid AM band interference and crosstalk
  - Optional clock synchronization
  - Switching frequency from 100 kHz to 2.2 MHz
  - Selectable switching mode (FPWM, diode emulation, and skip mode)
- EMI mitigation
  - Optional programmable spread spectrum
- Programmability and flexibility
  - Programmable wake-up and sleep threshold
  - Dynamic switching frequency programming
  - Adjustable soft start time
  - Adjustable output using 0.8 V ±1% reference
  - Adaptive dead-time control
- Integrated protection features
  - Overcurrent protection
    - Cycle-by-cycle peak current limit
    - Optional hiccup mode protection (buck)
    - Optional latch-off mode protection (buck)
  - Overvoltage protection
  - HB-SW short protection (boost)
  - Thermal shutdown

2 Applications

- Automotive infotainment / cluster
- Automotive body electronics / lighting
- Automotive ADAS

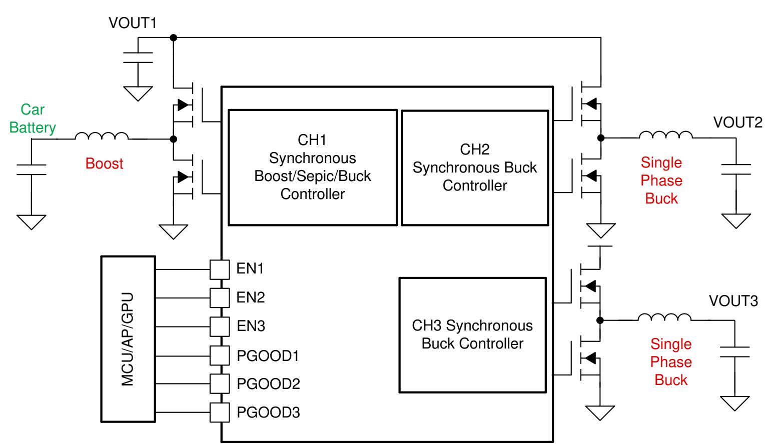
3 Description

The LM5127-Q1 is a full featured, wide input range three channel DC/DC controller which supports flexible topology (Boost/Buck) with peak current mode control. The device is designed as an integrated one-chip solution for the front-stage power supply in automotive infotainment, cluster, body control as well as ADAS systems. (continue on next page)

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM5127-Q1	QFN (48)	7.00 mm x 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application (Pre-boost + Two bucks)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (December 2020)	Page
• Changed device status from Advance Information to Production Data......	1

5 Description (continued)

The input voltage range covers both of automotive cold-cranking and load dump scenarios. The switching frequency is dynamically programmed in the range of 100 kHz to 2.2 MHz with an external resistor. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response.

The device features a low shutdown I_Q and an ultra-low I_Q sleep mode, which minimizes battery drain at no/light load condition and eliminates the need for an additional low I_Q LDO regulator as the CAN supply during standby.

The device includes flexible topology channels that support boost or SEPIC, and two independent single-phase bucks or a dual-phase buck to serve as a high current automotive processor supply. In boost mode, the device supports bypass operation which eliminates the need for an external bypass switch. In buck mode, the device supports low dropout operation to minimize dropout voltage. The battery monitor detects low battery voltage and signals when a backup process should start.

Minimal power dissipation is realized with a low current limit threshold and the use of an external VCC supply. The device has built-in protection features such as peak current limit which is constant over VIN, optional hiccup mode overload protection, overvoltage protection, and thermal shutdown.

External clock synchronization, programmable spread spectrum switching frequency, as well as a leadless package with minimal parasitics help to reduce EMI and avoid cross talk. Additional features include FPWM, DCR sensing, programmable soft start, a precision reference, and power-good indicators.

6 Pin Configuration and Functions

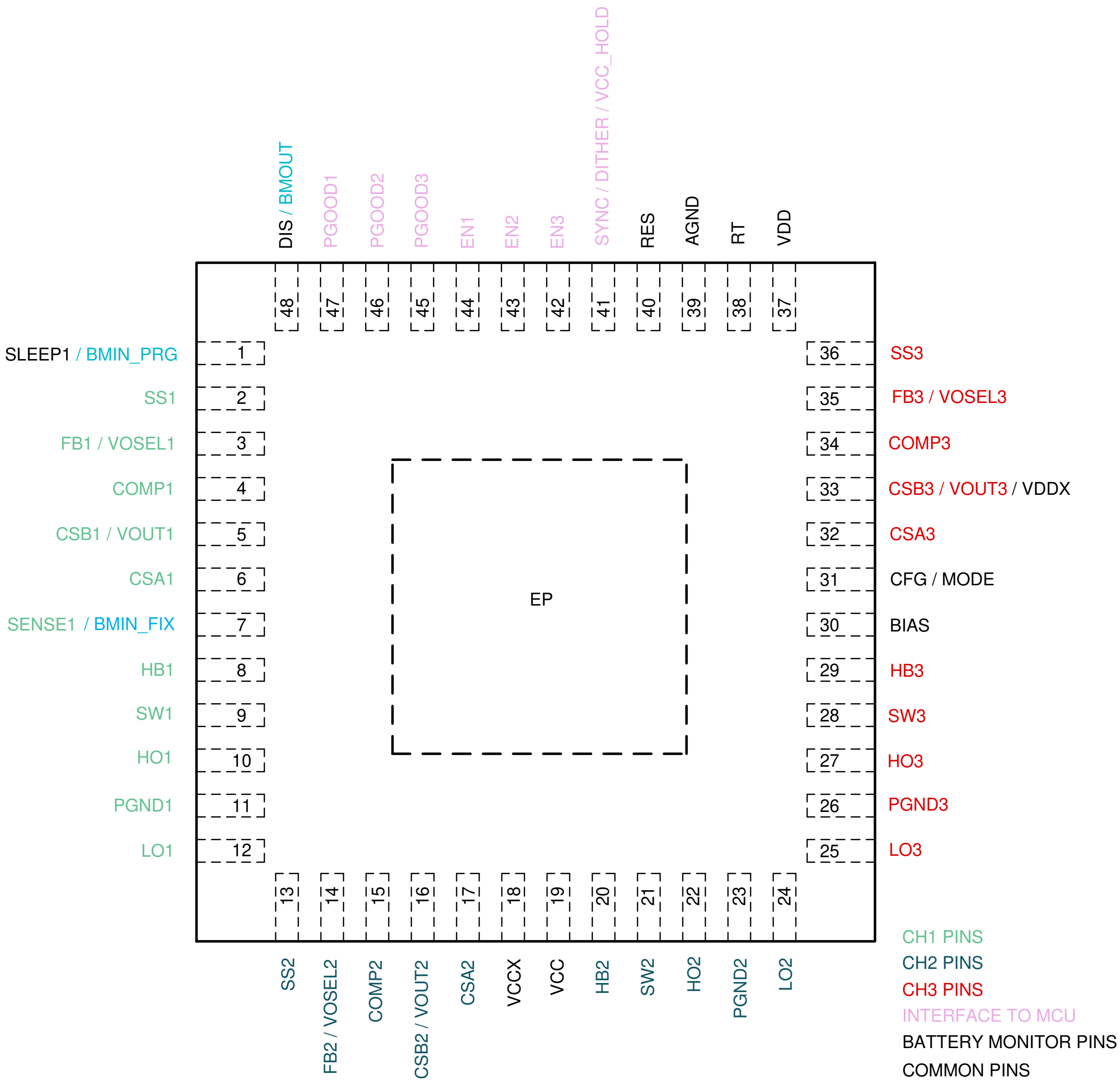


Figure 6-1. 48-pin QFN with Wettable Flanks RGZ Package (Top View)

Table 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
39	AGND	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
30	BIAS	P	Supply voltage input to the VCC regulator. Connect a 1-µF local BIAS capacitor from the pin to ground.
31	CFG/MODE	I	Device configuration (boost or buck, single-phase or dual-phase) and switching mode (FPWM or Skip mode) selection pin. Diode emulation mode is enabled by connecting 57.6 kΩ between SS and AGND in FPWM mode.
4	COMP1	O	Output of the internal trans-conductance error amplifier. Connect the loop compensation components between the pin and AGND.
15	COMP2		
34	COMP3		

Table 6-1. Pin Functions (continued)

PIN NO.	PIN NAME	I/O[(1)]	DESCRIPTION
6	CSA1	I	Current sense amplifier input pin. In boost configuration, the pin works as a negative input pin. In buck configuration, the pin works as a positive input pin.
17	CSA2		
32	CSA3		
5	CSB1/VOUT1	I	Current sense amplifier input pin. In boost configuration, the pin works as a positive input pin. In buck configuration, the pin works as a negative input pin and senses output voltage for fixed output voltage options. VDDX is an optional input for the VDD supply. If the VOUT3 regulation target is 3.3 V and the device is in deep sleep mode, VDDX is internally connected to VDD when VDD is less than 3.4 V (typical).
16	CSB2/VOUT2		
33	CSB3/VOUT3/VDDX		
48	DIS/BMOUT	O	When CH1 is configured as a pre-boost, the DIS pin works as a resistor divider disconnection pin. The pin is pulled low when at least one channel is in active mode. In order to minimize leak current through the resistor dividers, the pin opens during shutdown and during deep sleep mode when all enabled channels are in sleep, SLEEP1 > 1.02 V and SENSE1 > 6.0 V. When CH1 is configured as a buck, the pin works as a battery monitor output. The pin is pulled low when BMIN_FIX is less than 5.7 V or BMIN_PRG is less than 1.0 V. The pin opens when BMIN_FIX is greater than 6.0 V.
44	EN1	I	Enable pin. If EN is less than 0.4, the channel is in shutdown mode. The pin must be raised above 2.0 V to enable the channel. Connect to BIAS if not used.
43	EN2		
42	EN3		
3	FB1/VOSEL1	I	Error amplifier negative feedback input or fixed output voltage selection pin. In buck configuration, connect the pin to AGND for a 3.3-V output, connect the pin to VDD for a 5-V output, or connect feedback resistors to the pin to program the output regulation target. In boost configuration, always connect feedback resistors to the pin to program the output regulation target.
14	FB2/VOSEL2		
35	FB3/VOSEL3		
8	HB1	P	High-side driver supply for bootstrap gate drive. In boost configuration, boot diode is internally connected from VCC to the pin. Connect external boot diode from the pin to VCC in buck topology. Connect a 0.1-µF capacitor between the pin and SW. Connect HB to VCC directly for non-synchronous boost operation.
20	HB2		
29	HB3		
10	HO1	O	High-side gate driver output. Connect to the gate of the N-channel MOSFET through a short, low inductance path.
22	HO2		
27	HO3		
12	LO1	O	Low-side gate driver output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
24	LO2		
25	LO3		
11	PGND1	G	Power ground pin. Connect directly to the source of the N-channel MOSFET through a short, low inductance path.
23	PGND2		
26	PGND3		
47	PGOOD1	O	Power-good indicator with open-drain output. In buck configuration, the pin is pulled low when VOUT is out of the regulation window. In boost configuration, the pin is pulled low when VOUT is less than the regulation target.
46	PGOOD2		
45	PGOOD3		
40	RES	O	Restart timer pin. A capacitor between RES and AGND determines the time the channel remains off before automatically restarting in hiccup mode. If the pin is connected to AGND, the channel never restarts after the hiccup mode off-time until EN is toggled. If the pin is connected to VDD during initial power-on, the hiccup mode fault counter is disabled and the device operates with non-hiccup mode cycle-by-cycle current limit. The fault counter of each channel operates independently. One channel can operate in normal mode while the other is in hiccup mode overload protection.
38	RT	I/O	Switching frequency setting pin. If no external clock is applied to SYNC, the switching frequency is programmed by a single resistor between RT and AGND.
7	SENSE1/BMIN_FIX	I	When CH1 is configured as a synchronous boost, SENSE1 senses the output voltage. The pin should be connected to the drain connection of the high side MOSFET as close as possible in boost configuration. When CH1 is configured as a buck, BMIN_FIX works as a fixed threshold battery monitor input pin.

Table 6-1. Pin Functions (continued)

PIN		I/O[(1)]	DESCRIPTION
NO.	NAME		
1	SLEEP1/BMIN_PRG	I	When CH1 is configured as a boost, it is allowed to enter sleep mode when SLEEP1 is greater than 1.0 V. When CH1 is configured as a buck, BMIN_PRG works as a programmable threshold battery monitor input pin.
2	SS1	I/O	Soft-start time programming pin. The device forces diode emulation during soft-start time. By connecting 57.6 kΩ to ground in FPWM mode, the device works in diode emulation without entering sleep mode. Switching stops when SS is grounded.
13	SS2		
36	SS3		
9	SW1	P	Switching node. Connect directly to the source of the high-side MOSFET and the drain of the low-side MOSFET through a short, low inductance path. Connect SW to PGND directly for non-synchronous boost operation.
21	SW2		
28	SW3		
41	SYNC/DITHER / VCC_HOLD	I/O	External synchronization clock input or dithering frequency programming pin. The internal oscillator can be synchronized to an external clock during the operation. If VCC_HOLD > 2.0 V, the device holds the VCC pin voltage higher than VCC UVLO threshold when all EN pins are grounded, which helps to restart switching immediately without reconfiguration. If a capacitor is connected between the pin and AGND, dithering is enabled. In this mode, the capacitor is charged and discharged with a 20-µA current source/sink. As the voltage on the pin ramps up and down, the oscillator frequency is modulated between –7% and +7% of the nominal frequency set by the RT resistor. Dithering can be disabled during the operation by pulling down the pin to ground. Connect the pin to AGND if the pin is not used.
19	VCC	P	VCC bias supply pin. Connect a 10-µF VCC capacitor between the pin and power ground.
18	VCCX	P	Optional input for an external VCC supply. If VCCX > 4.5 V, VCCX is internally connected to VCC. Connect a 0.47-µF local VCCX capacitor between the pin and PGND. If VCCX is unused, the pin must be connected to ground.
37	VDD	P	VDD bias supply pin. Connect a 0.1-µF VDD capacitor between the pin and AGND.
-	EP		Exposed pad of the package. EP is internally connected to AGND. EP must be soldered to the large analog ground plane to reduce thermal resistance.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range(1)

		MIN	MAX	UNIT
Input(4)	BIAS, SENSE1 to AGND	–0.3	50	V
	DIS, FB1, SLEEP1 to AGND	–0.3	SENSE1+0.3	
	ENx to AGND	–0.3	BIAS+0.3	
	VCCX to AGND	–0.3	5.8(2)	
	SWx to AGND (50ns)	–1		
	HBx to AGND	–0.3	50	
	HBx to SWx	–0.3	5.8(2)	
	HB1 to BIAS		40	
	CSBx to AGND	–0.3	50	
	CSAx to CSBx	–0.3	0.3	
	CFG, FB2, FB3 to AGND	–0.3	5.5	
	SYNC, RES, RT to AGND	–0.3	VDD+0.3	
	PGNDx to AGND	–0.3	0.3	
Output(4)	HOx to SWx (50ns)	–1		V
	LOx to PGND (50ns)	–1		
	VCC, VDD to AGND	–0.3	5.8(2)	
	PGOODx(5), SSx, COMPx to AGND	–0.3	5.5	
Junction temperature, T_J (3)		–40	150	°C
Storage temperature, T_{STG}		–55	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operating lifetime is de-rated when the pin voltage is greater than 5.5V.
(3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.
(4) It is not allowed to apply an external voltage to the COMPx, SSx, RT, CFG, LOx, HOx pins.
(5) The maximum current sink is limited to 1 mA when $V_{PGOOD} > V_{BIAS}$

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range [(1)]

		MIN	NOM	MAX	UNIT
$V_{SUPPLY(BOOST)}$	Boost converter input (when BIAS ≥ 3.8V)	0.8		42	V
$V_{LOAD(BOOST)}$	Boost converter output			42	V
$V_{SUPPLY(BUCK)}$	Buck converter input			42	V
$V_{LOAD(BUCK)}$	Buck converter output	0.8		42	
V_{BIAS}	BIAS input	3.8		42	V
V_{VCCX}	VCCX input	4.5		5.25	V
V_{EN}	Enable input	0		42	V
V_{SYNC}	Synchronization pulse input	0		5.25	V
V_{CSA1}, V_{CSB1}, V_{CSA2}, V_{CSB2}, V_{CSA3}, V_{CSB3}	Current sense input	0		42	V
V_{SENSE1}	Boost output sense, battery monitor input	0		42	V
V_{FB}	Feedback input (FB1)	0		42	V
V_{FB}	Feedback input (FB2, FB3)	0		5.25	V
F_{SW}	Typical switching frequency	100		2200	kHz
F_{SYNC}	Synchronization pulse frequency	200		2200	kHz
T_J	Operating junction temperature[(2)]	–40		150	°C

(1) Operating Ratings are conditions under the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

7.4 Thermal Information

THERMAL METRIC[(1)]		LM5127-Q1	UNIT
		RGZ (QFN)	
		48 PINS	
R_{qJA}	Junction-to-ambient thermal resistance (LM5127EVM) [(2)]	28.9	°C/W
R_{qJA}	Junction-to-ambient thermal resistance	31.8	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	21.9	°C/W
R_{qJB}	Junction-to-board thermal resistance	13.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (LM5127EVM) [(2)]	0.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (LM5127EVM) [(2)]	13.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	12.9	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Applicable only to the EVM with no airflow.

7.5 Electrical Characteristics

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT(BIAS, VCCX, VDDX)						
$I_{BIAS-SD}$	BIAS current in shutdown (VCCX=0V)	V_{EN1} = 0 V, V_{EN2} = 0 V, V_{EN3} = 0 V, V_{VCC_HOLD} = 0 V		2.8	4.5	µA
$I_{BATTERY-SLEEP}$	Battery drain in deep sleep mode ($V_{BATTERY}$ = 12 V, VCCX = 5 V (CH2), VDDX = 3.3 V (CH3), Non-switching)	V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 boost mode		33		µA
		V_{EN1} = 0 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 boost mode		22		µA
		V_{EN1} = 0 V, V_{EN2} = 2.5 V, V_{EN3} = 0 V, CH1 boost mode		20		µA
		V_{EN1} = 0 V, V_{EN2} = 0 V, V_{EN3} = 2.5 V, CH1 boost mode		14		µA
		V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 buck mode		32		µA
$I_{BIAS-SLEEP1}$	BIAS current in sleep mode (VDDX = 3.3 V, VCCX = 5 V)	V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 boost mode		2.0		µA
$I_{BIAS-SLEEP2}$	BIAS current in sleep mode (VDDX = 0 V, VCCX = 0 V)	V_{EN1} = 0 V, V_{EN2} = 0 V, V_{EN3} = 0 V, V_{VCC_HOLD} = 2.5 V, CH1 buck mode		25	38	µA
$I_{VDDX-SLEEP}$	VDDX current in sleep mode (VDDX = 3.3 V, VCCX = 0 V)	V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 boost mode		100	115	µA
$I_{BIAS-ACTIVE1}$	BIAS current in active mode (VCCX = 0 V)	V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 boost mode		3300	3900	µA
		V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 0 V, CH1 boost mode		2400	2850	µA
		V_{EN1} = 2.5 V, V_{EN2} = 0 V, V_{EN3} = 0 V, CH1 buck mode		1700	2000	µA
$I_{BIAS-ACTIVE2}$	BIAS current in active mode (VCCX = 5 V)	V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 2.5 V, CH1 boost mode		125	175	µA
		V_{EN1} = 2.5 V, V_{EN2} = 2.5 V, V_{EN3} = 0 V, CH1 boost mode		125	175	µA
		V_{EN1} = 2.5 V, V_{EN2} = 0 V, V_{EN3} = 0 V, CH1 buck mode		125	175	µA
ENABLE(EN1, EN2, EN3)						
$V_{EN-RISING}$	Enable threshold (ENx)	EN rising			2	V
$V_{EN-FALLING}$	Enable threshold(ENx)	EN falling	0.4			V
SLEEP1 in BOOST, BMIN_PRG in Buck						
$V_{SLEEP1-FALLING}$	SLEEP1/BMIN_PRG threshold	SLEEP1 falling	0.95	1	1.05	V
$V_{SLEEP1-HYS}$	SLEEP1/BMIN_PRG hysteresis	SLEEP1 rising		15		mV
I_{SLEEP1}	Hysteresis current (current sink)			30		µA
$t_{D-WAKE1}$	Wakeup delay	SENSE1 falling to DIS falling			5	µs
BMIN_FIX in Buck						
$V_{BMIN\_FIX-FALLING}$	BMIN_FIX threshold	BMIN_FIX falling	5.415	5.7	5.985	V
$V_{BMIN\_FIX-RISING}$	BMIN_FIX threshold	BMIN_FIX rising	5.7	6.0	6.3	V
I_{BMIN_FIX}	BMIN_FIX bias current	V_{BMIN1} = 12 V		1	3	µA
VCC and VCCX						
$V_{VCC-REG}$	VCC regulation	V_{BIAS} = 7.0 V, I_{VCC} = 250 mA	4.75	5	5.25	V
	VCC regulation	V_{BIAS} = 7.0 V, no load	4.75	5	5.25	V

7.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VCC regulation during dropout	V_{BIAS} = 3.8 V, I_{VCC} = 250 mA	3.42			V
$V_{VCC\text{-}UVLO\text{-}RISING}$	VCC UVLO threshold	VCC rising	3.55	3.65	3.75	V
$V_{VCC\text{-}UVLO\text{-}FALLING}$	VCC UVLO threshold	VCC falling	3.2	3.3	3.4	V
$I_{VCC\text{-}CL}$	VCC sourcing current limit	VCC = 4 V	250			mA
$V_{VCCX\text{-}RISING}$	VCCX transition threshold	VCCX rising	4.2	4.3	4.4	V
$V_{VCCX\text{-}FALLING}$	VCCX transition threshold	VCCX falling	4.0	4.1	4.2	V
	VCCX to VCC dropout	V_{VCCX} = 4.5 V, I_{VCC} = 250 mA	4.2			V
VDD and VDDX						
$V_{VCC\text{-}REG}$	VDD regulation	V_{BIAS} = 7.0 V, No load at VCC, VCCX=GND	4.75	5	5.25	V
$V_{VDD\text{-}UVLO\text{-}RISING}$	VDD UVLO threshold	VDD rising	3.0	3.1	3.2	V
$V_{VDD\text{-}UVLO\text{-}FALLING}$	VDD UVLO threshold	VDD falling	2.9	3	3.1	V
SYNC/DITHER/VCC_HOLD						
$V_{SYNC\text{-}RISING}$	SYNC threshold/SYNC detection threshold	SYNC rising			2	V
$V_{SYNC\text{-}FALLING}$	SYNC threshold	SYNC falling	0.4			V
	Minimum SYNC pulse width				100	ns
I_{DITHER}	Dither source/sink current		16	20	24.5	µA
Δf_{SW1}	f_{SW} Modulation (Upper Limit)			+7		%
Δf_{SW2}	f_{SW} Modulation (Lower Limit)			-7		%
$V_{DITHER\text{-}FALLING}$	Dither disable threshold		0.65	0.75	0.85	V
RT						
V_{RT}	RT regulation			0.5		V
DISCONNECTION(DIS), BATTERY MONITOR OUTPUT(BMOUT)						
r_{DIS}	DIS pulldown switch $r_{DS(on)}$			17	34	Ω
SS						
I_{SS1}	Soft-start current	SS < 1.0 V	17	20	23	µA
I_{SS2}	Soft-start current	SS>1.5V		2		µA
$r_{SS\text{-}PD}$	SS pulldown switch $r_{DS(on)}$			50	93	Ω
$V_{SS\text{-}DONE}$	MODE transition	SS rising		1.5		V
$V_{SS\text{-}DIS}$	SS discharge detection threshold		50	75	105	mV
PULSE WIDTH MODULATION(PWM)						
f_{SW1}	Switching frequency	R_T = 220 kΩ	85	100	115	kHz
f_{SW2}	Switching frequency	R_T = 9.09 kΩ	1980	2200	2420	kHz
$t_{ON\text{-}MIN\text{-}BUCK}$	Minimum controllable on-time (HO on-time in Buck)	R_T = 9.09 kΩ	12	20	31	ns
$t_{OFF\text{-}MIN\text{-}BUCK}$	Minimum HO off-time during dropout (Buck)	R_T = 9.09 kΩ	85	110	150	ns
$t_{ON\text{-}MIN\text{-}BOOST}$	Minimum controllable on-time (LO on-time in Boost)	R_T = 9.09 kΩ		25		ns
$t_{OFF\text{-}MIN\text{-}BOOST}$	Minimum controllable off-time (LO off-time in Boost)	R_T = 9.09 kΩ	70	90	118	ns
$D_{MAX\text{-}BOOST1}$	Maximum duty cycle limit in Boost mode	R_T = 220kΩ	90	94	98	%
$D_{MAX\text{-}BOOST2}$	Maximum duty cycle limit in Boost mode	R_T = 9.09 kΩ	75	80	83	%

7.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Max pulse skip in low dropout mode			16		cycles
LOW IQ SLEEP MODE						
$V_{WAKE-FB}$	FB wakeup threshold	In reference to V_{REF}		–1		%
$V_{WAKE-COMP}$	COMP wakeup threshold			316		mV
$t_{D-WAKE2}$	Wake-up delay	R_T = 9.09 kΩ		4.4		µs
$V_{MINCLTH}$	Minimum peak current in skip mode	Current sense input		10		mV
CURRENT SENSE (CSPx, CSNx)						
V_{SLOPE}	Peak slope compensation amplitude	R_T = 220 kΩ, in reference to CS inputs		80		mV
A_{CS}	Current sense amplifier gain			10		V/V
V_{CLTH1}	Positive peak current limit threshold (CS input)	CSBx = 3.3 V in Buck	52	60	68	mV
V_{CLTH2}	Positive peak current limit threshold (CS input)	CSBx = 0 V in Buck	48	60	69	mV
I_{CSA}	CSA bias current				1	µA
I_{CSB}	CSB bias current			120		µA
	CS amplifier switch over			2.5		V
HICCUP MODE PROTECTION (RES)						
	Fault counter timeout			256		cycles
	Normal cycles to reset fault counter			8		cycles
I_{RES}	RES current source		16	20	24	µA
V_{RESTH}	RES threshold		0.95	1.0	1.05	V
R_{RES}	RES pulldown switch $r_{DS(on)}$			20	40	Ω
$V_{RES-DIS}$	RES discharge detection			100		mV
ERROR AMPLIFIER (COMPx, FBx)						
$V_{OUT-REG1}$	VOUT regulation (3.3 V)		3.26	3.3	3.34	V
$V_{OUT-REG2}$	VOUT regulation (5.0V)		4.94	5.0	5.06	V
V_{REF}	Error amplifier reference	In Boost	0.788	0.8	0.812	V
V_{REF}	Error amplifier reference	In Buck	0.792	0.8	0.808	V
Gm	Transconductance			1		mA/V
$I_{SOURCE-MAX}$	Maximum COMP sourcing current	V_{COMP} = 0 V	80			µA
$I_{SINK-MAX}$	Maximum COMP sinking current	V_{COMP} = 2.2 V	80			µA
$V_{CLAMP-MAX}$	COMP clamp voltage	COMP rising	2.6			V
V_{OFFSET}	COMP to PWM input offset		0.264	0.300	0.336	V
V_{FB-SS}	Internal FB to SS clamp	V_{FB} = 0 V		80	115	mV
PGOOD, OVP						
$V_{OVTH-RISING}$	Overvoltage threshold (OVP in Buck)	FB rising (In reference to V_{REF})	105	107	109	%
$V_{OVTH-FALLING}$	Overvoltage threshold (OVP in Buck)	FB falling (In reference to V_{REF})	103	105	107	%
$V_{UVTH-RISING}$	Undervoltage threshold	FB rising (In reference to V_{REF})	93	95	97	%
$V_{UVTH-FALLING}$	Undervoltage threshold	FB falling (In reference to V_{REF})	91	93	95	%

7.5 Electrical Characteristics (continued)

Typical values correspond to T_J=25°C. Minimum and maximum limits apply over T_J=-40°C to 125°C. Unless otherwise stated, V_{BIAS} = 12 V, R_T = 9.09 kΩ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	PGOOD deglich filter	Both edges		23		µs
R_{PGOOD}	PGOOD pulldown switch R_{DSON}			42	82	Ω
MOSFET DRIVER, SENSE1						
V_{HO-H}	High-state voltage drop (HO driver)	100-mA sinking		0.1	0.15	V
V_{HO-L}	Low-state voltage drop (HO driver)	100mA sourcing		0.05	0.1	V
V_{LO-H}	High-state voltage drop (LO driver)	100-mA sinking		0.1	0.15	V
V_{LO-L}	Low-state voltage drop (LO driver)	100-mA sourcing		0.05	0.1	V
$V_{HB-UVLO-FALLING}$	HB-SW UVLO threshold	HB-SW falling	2.2	2.50	2.75	V
$I_{HB-SLEEP}$	HB quiescent current in sleep	HB-SW = 5 V		3.5	7	µA
t_{DHL}	HO off to LO on deadtime		12	22	35	ns
t_{DLH}	LO off to HO on deadtime		12	22	35	ns
$V_{ZCD-BOOST}$	SENSE1 to SW ZCD threshold for boost			6		mV
$V_{ZCD-BUCK}$	SW to PGND ZCD threshold for buck			–5		mV
I_{CHG}	Charge pump current	BIAS = 3.8 V	10			µA
THERMAL SHUTDOWN						
$T_{TSD-RISING}$	Thermal shutdown threshold	Temperature rising		175		°C
$T_{TSD-HYS}$	Thermal shutdown hysteresis			15		°C

7.6 Typical Characteristics

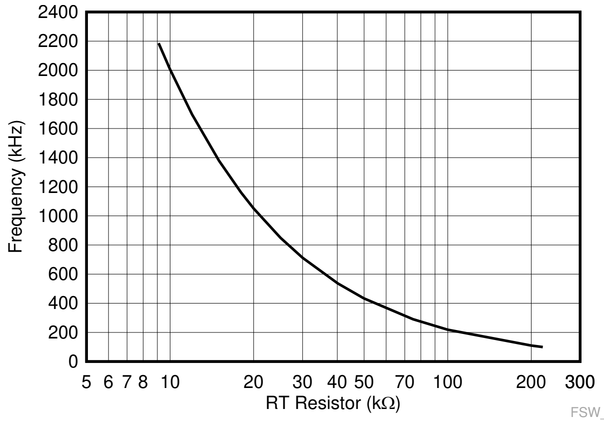


Figure 7-1. Frequency vs RT Resistance

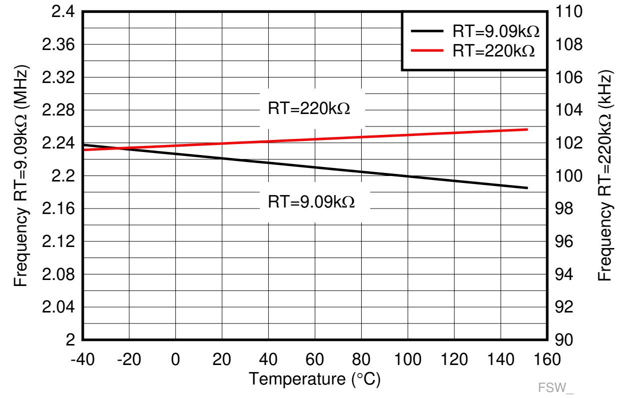


Figure 7-2. Frequency vs Temperature

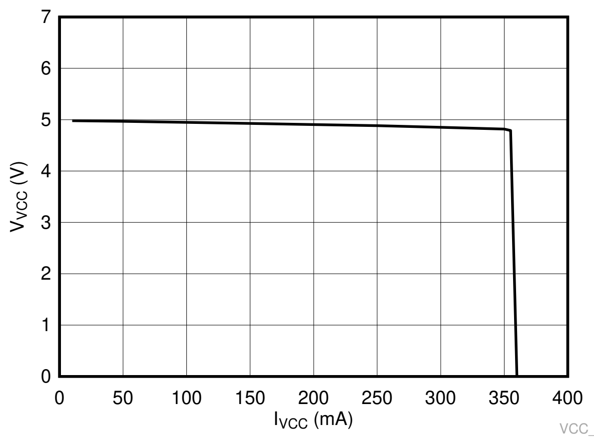


Figure 7-3. V_{VCC} vs I_{VCC}

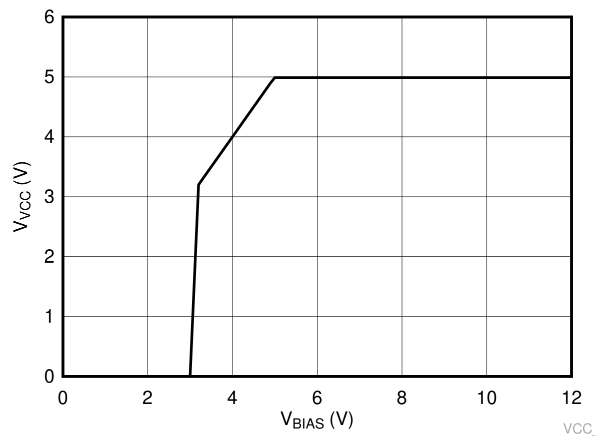


Figure 7-4. V_{VCC} vs V_{BIAS} (No Load)

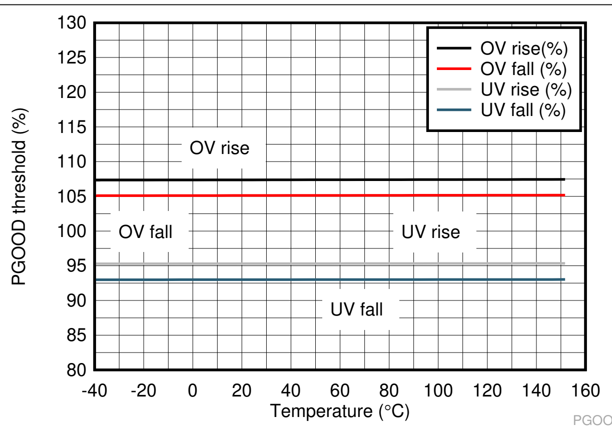


Figure 7-5. PGOOD Threshold (V_{OVTH} , V_{UVTH}) vs Temperature

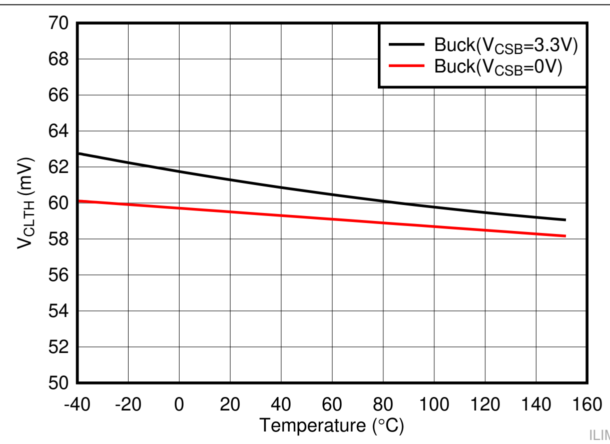


Figure 7-6. Current Limit Threshold vs Temperature

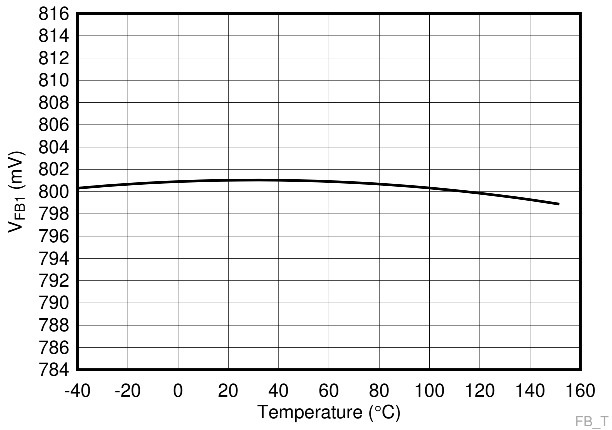


Figure 7-7. FB Reference vs Temperature

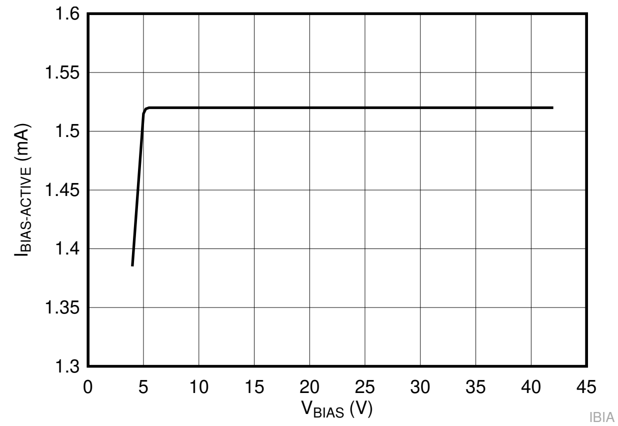


Figure 7-8. $I_{BIAS-ACTIVE}$ vs V_{BIAS}(One Channel)

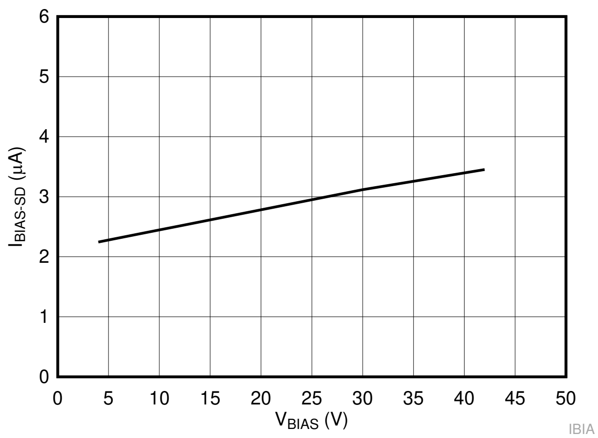


Figure 7-9. $I_{BIAS-SD}$ vs V_{BIAS}

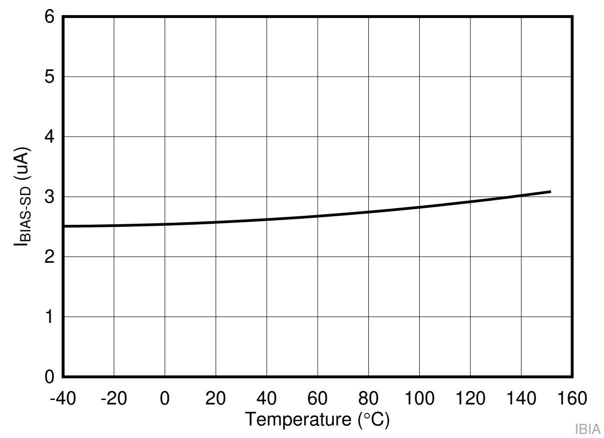


Figure 7-10. $I_{BIAS-SD}$ vs Temperature

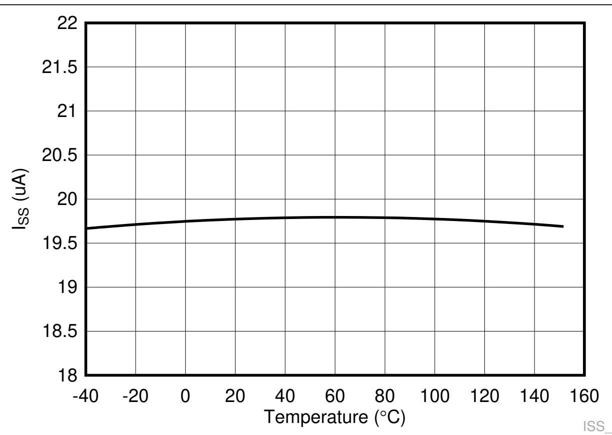


Figure 7-11. I_{SS} vs Temperature

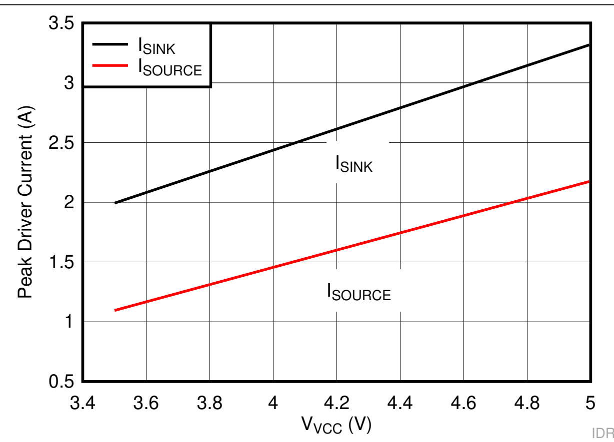


Figure 7-12. Peak Driver Current vs VCC

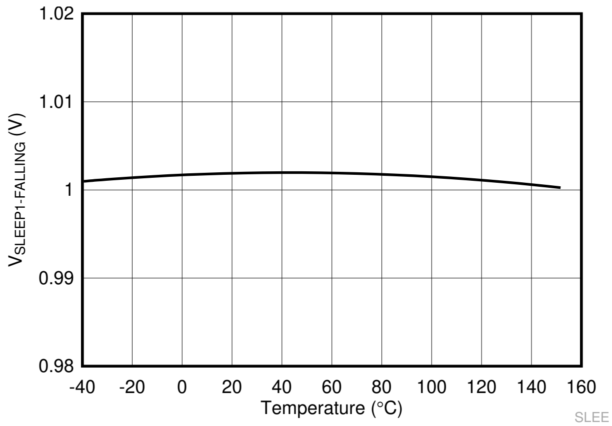


Figure 7-13. SLEEP1 Threshold vs Temperature

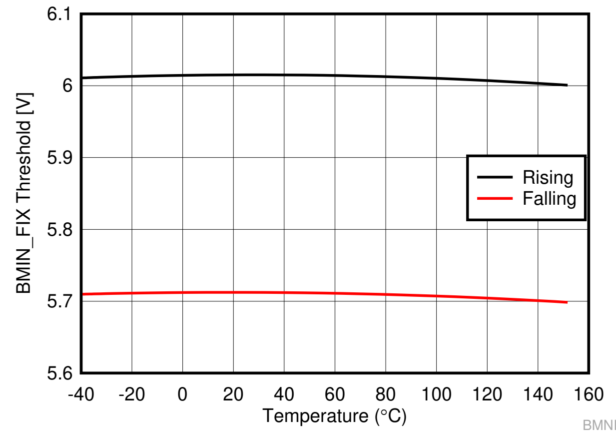


Figure 7-14. BMIN_FIX (Rising, Falling) vs Temperature

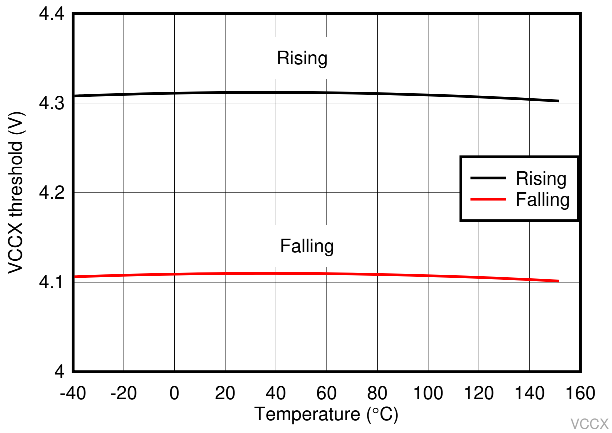


Figure 7-15. VCCX Transition Threshold (Rising, Falling) vs Temperature

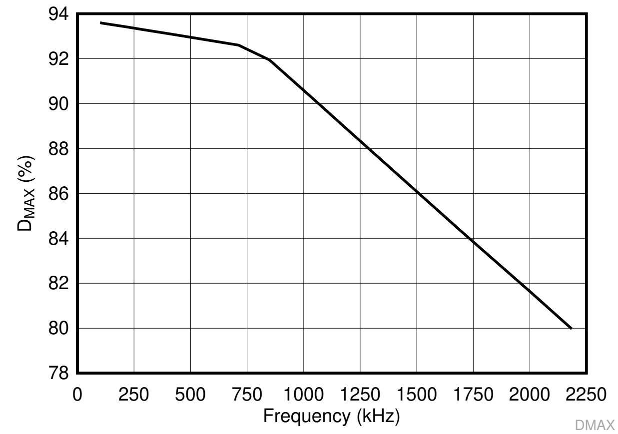


Figure 7-16. D_{MAX} vs Frequency

8 Detailed Description

8.1 Overview

The LM5127-Q1 is a full featured, wide input range three channel DC/DC controller which supports flexible topology (Boost/Buck) with peak current mode control. The device is designed as an integrated one-chip solution for the front-stage power supply in automotive infotainment, cluster, body control, as well as ADAS systems.

The input voltage range covers automotive cold-cranking and load dump scenarios. The switching frequency is dynamically programmed in the range of 100 kHz to 2.2 MHz with an external resistor. Switching at 2.2 MHz minimizes AM band interference and allows for a small solution size and fast transient response.

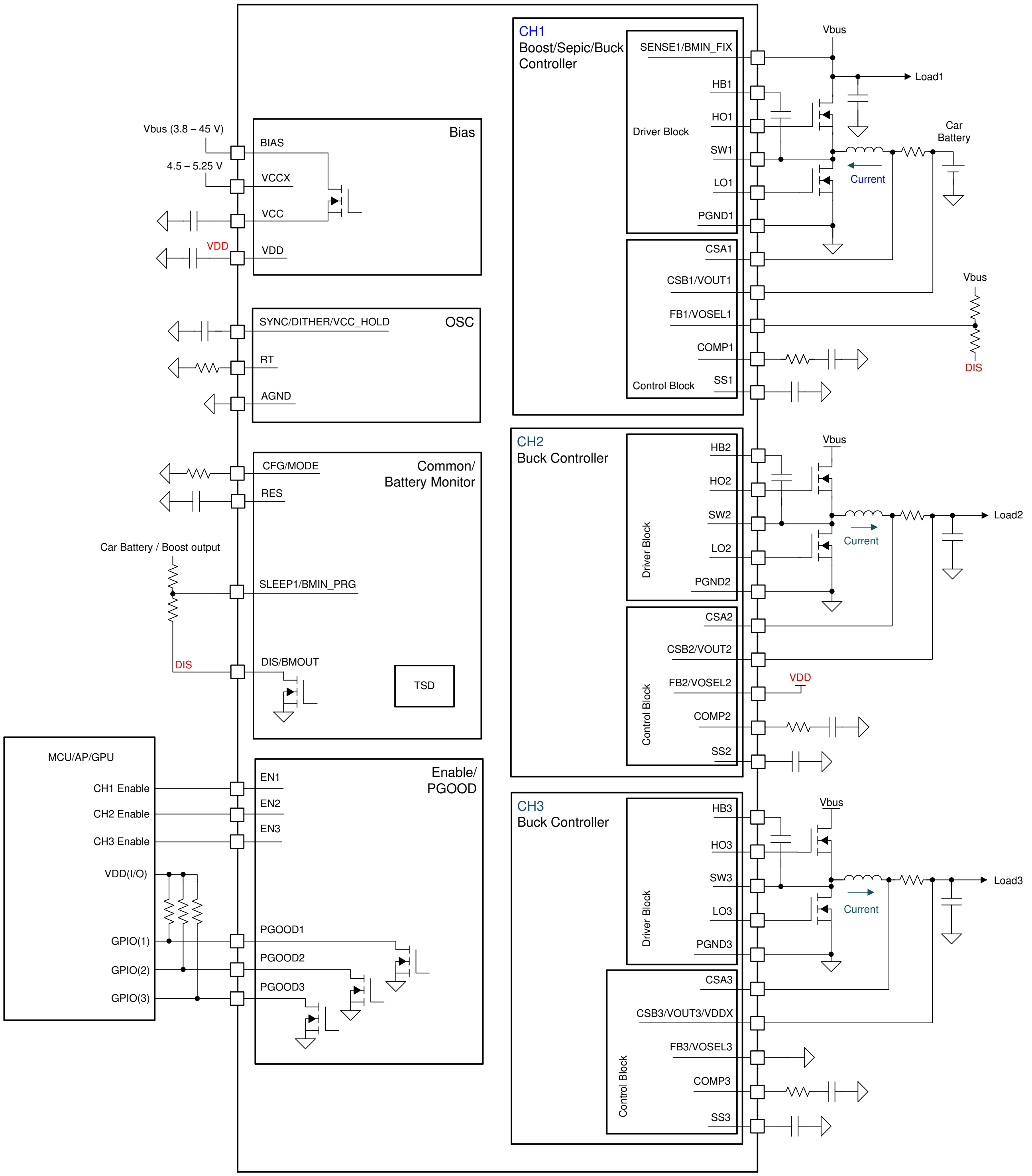
The device features a low shutdown I_Q and an ultra-low I_Q sleep mode, which minimizes battery drain at no/light load condition and eliminates the need for an additional low I_Q LDO regulator as the CAN supply during standby.

The device includes flexible topology channels that support boost or SEPIC, and two independent single-phase bucks or a dual-phase buck to serve as a high current automotive processor supply. In boost mode, the device supports bypass operation which eliminates the need for an external bypass switch. In buck mode, the device supports low dropout operation to minimize dropout voltage. The battery monitor detects low battery voltage and signals when a backup process should start.

Minimal power dissipation is realized with a low current limit threshold and the use of an external VCC supply. The device has built-in protection features such as peak current limit which is constant over VIN, optional hiccup mode overload protection, overvoltage protection, and thermal shutdown.

External clock synchronization, programmable spread spectrum switching frequency, as well as a leadless package with minimal parasitics help to reduce EMI and avoid cross talk. Additional features include FPWM, DCR sensing, programmable soft start, a precision reference, and power-good indicators.

8.2 Functional Block Diagram



8.3 Feature Description

Note

Please take a quick read through Section 8.4 before reading the detailed descriptions of the device. It is recommended to understand which device statuses and what type of light load switching modes are supported by the device.

The parameters or thresholds values mentioned in this section are reference values unless otherwise specified. Please refer to Section 7.5 to find the ensured minimum, maximum, and typical values.

8.3.1 Device Enable (EN, VCC_HOLD)

The device is enabled when at least one of the EN pins is greater than the EN threshold (V_{EN}), or VCC_HOLD is greater than the SYNC threshold (V_{SYNC}), and the device shuts down when all the EN pins are less than V_{EN} and the VCC_HOLD pin is less than V_{SYNC}. When enabled, the device turns on the internal VCC regulator and VCC-to-VDD switch after a 40-µs delay, and begins an initial configuration when VDD is greater than 3.1 V. The device is fully enabled after a 130-µs initial configuration time.

After the initial configuration ends, the EN pins work as independent enable pins for each channel. If the EN pin is pulled down below V_{EN}, the applicable channel stops switching, grounds the SS and PGOOD pins, and discharges the COMP pin.

The EN pins have an internal 0.5-µA pulldown current sink to prevent a false turnon. Connect an external pulldown resistor if a stronger pulldown is required. The EN pins also have an internal diode path to the BIAS pin. By adding a 5-kΩ resistor at the EN pin, the EN pin can be supplied before the BIAS pin is biased. If the EN pin is not controlled by user input, connect the EN pin to the BIAS pin.

8.3.2 Dual Input VCC Regulator (BIAS, VCCX, VCC)

The device features a dual input VCC regulator which is sourced from either the BIAS pin or the VCCX pin. The VCC regulator is enabled 40 µs after the device is enabled.

The high voltage VCC regulator allows connecting the BIAS pin directly to supply voltages from 3.8 V to 47 V. When the BIAS pin voltage is greater than the 5-V VCC regulation target ($V_{VCC\text{-}REG}$), the VCC regulator provides the 5-V regulated output. When the BIAS pin voltage is below $V_{VCC\text{-}REG}$ and VCCX is not used, the VCC output tracks the BIAS pin voltage with a small dropout.

The minimum VCC regulator current limit is 250 mA ($I_{VCC\text{-}CL}$) during the initial configuration or when the device is in active mode. The 5-V gate charge of the external power MOSFET ($Q_{G@5V}$) should be selected to satisfy the following inequality.

$$6 \times Q_{G@5V} \times f_{SW} < I_{VCC\text{-}CL} \quad (1)$$

The VCC regulator current limit is reduced to 1 mA in deep sleep mode, or when the all EN pins are less than V_{EN} while VCC_HOLD is greater than V_{SYNC}. The recommended minimum VCC capacitor (C_{VCC}) value is 10 µF.

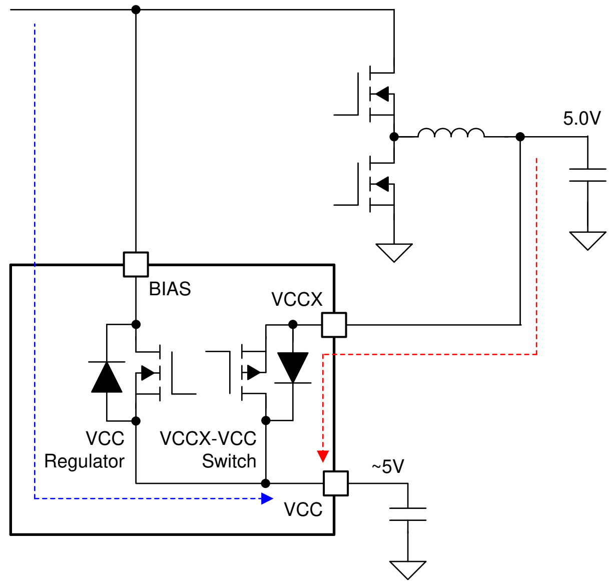


Figure 8-1. Dual Input VCC Regulator

The battery drain in deep sleep mode and the internal power dissipation of the VCC regulator can be minimized by connecting the VCCX pin to an external power source which is greater than 4.5 V and less than 5.5 V. The VCC regulator is disabled when the VCCX pin is greater than the VCCX transition threshold (V_{VCCX}). The internal VCCX-to-VCC switch is on when the VCC pin voltage is less than the VCCX pin voltage. If the 5-V buck output is connected to the VCCX pin, the 5-V output should be well regulated within ±10% tolerance during a load transient.

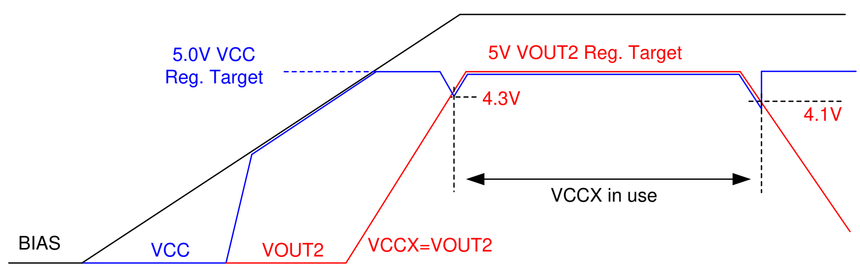


Figure 8-2. BIAS to VCCX Transition when VCCX = VOUT2 = 5 V

The VCCX-to-VCC switch has no active current limit. Also, if VCCX is greater than BIAS + 0.6 V, an external reverse blocking diode is required between the input power supply and the BIAS pin. The external reverse blocking diode prevents the external VCCX supply from passing current to the BIAS pin through the VCC regulator and the VCCX-to-VCC switch. The external VCCX supply voltage can be greater than the BIAS pin voltage without the external blocking diode only if the external VCCX supply is current limited to less than 200 mA. If VCCX is not used, the VCCX pin must be grounded.

The device provides a 130 µs $V_{VCC\text{-}UVLO\text{-}RISING}$-to-switching delay to ensure C_{VCC} is fully charged by the VCC regulator before switching. If the 130-µs delay is not enough because the BIAS pin voltage rises slowly, an external RC filter can be added to the EN pin to enable the device when the BIAS pin voltage is enough high.

If CH1 is configured as a boost and the bypass operation is required, the BIAS pin should be connected to the output of the boost converter. By connecting the BIAS pin to the output of the boost converter, the start-up voltage of the boost converter is affected since the boost converter output is the converter input voltage minus one diode voltage drop before start-up, but once the converter starts up, the device allows 0.8-V minimum boost input voltage. See *Section 8.3.16* for more detailed information.

8.3.3 Dual Input VDD Switch (VDD, VDDX)

The device also features a dual input VDD which is sourced from the VDD pin or the VDDX pin.

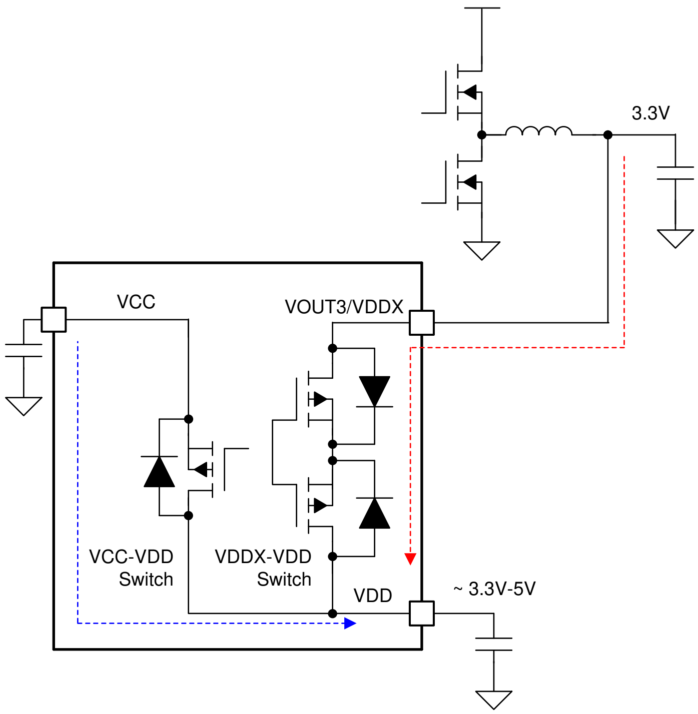


Figure 8-3. Dual Input VDD and Internal VDD Switches

The battery drain in deep sleep mode is also minimized by using the VDDX pin. When VOUT3 is configured to fixed 3.3 V, the VCC-to-VDD switch is off in deep sleep mode, and the VDDX-to-VDD switch is on when the VDD pin voltage is less than 3.4 V. The recommended VDD capacitor (C_{VDD}) value is 0.1 µF or greater.

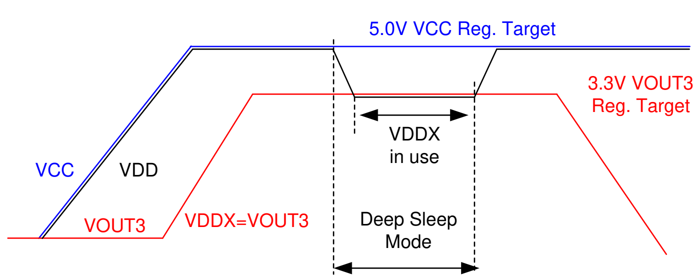


Figure 8-4. VCC to VDDX Transition when VDDX=VOUT3 = 3.3V

8.3.4 Device Configuration and Light Load Switching Mode Selection (CFG/MODE)

During the initial configuration period, the device configuration and the light load switching mode are programmed with an external resistor connected between CFG and AGND. The device configuration starts when the VDD pin voltage is greater than 3.1 V. To reset and reconfigure the device, all the EN pins and the VCC_HOLD pin should be less than V_{EN} and V_{SYNC}, respectively, or VCC must be fully discharged. The preferred way to reconfigure the device is to toggle all three EN and VCC_HOLD pins together.

Table 8-1. Device Configuration and Mode Selection

<table>
<tr><th rowspan="2">#</th><th rowspan="2">R_{CFG} (1)</th><th colspan="4">CONFIGURATION</th><th colspan="2">MODE</th></tr>
<tr><th>CH1</th><th>CH2</th><th>CH3</th><th>BATTERY MONITOR</th><th>LIGHT LOAD SWITCHING MODE(2)</th><th>DEEP SLEEP MODE(3)</th></tr>
<tr><td>1</td><td>GND</td><td>Boost</td><td rowspan="4">Single Buck</td><td rowspan="4">Single Buck</td><td>N/A</td><td rowspan="2">Skip Mode</td><td rowspan="2">All enabled channels should be in sleep. VCCX or VDDX should be in use.</td></tr>
<tr><td>2</td><td>9.53 kΩ</td><td>Buck</td><td>Available</td></tr>
<tr><td>3</td><td>19.1 kΩ</td><td>Boost</td><td>N/A</td><td rowspan="2">FPWM/DE Mode</td><td rowspan="2">N/A</td></tr>
<tr><td>4</td><td>29.4 kΩ</td><td>Buck</td><td>Available</td></tr>
<tr><td>5</td><td>41.2 kΩ</td><td>Boost</td><td colspan="2" rowspan="4">Dual-phase Buck</td><td>N/A</td><td rowspan="2">CH1 : Skip Mode
CH2,CH3 : FPWM/DE Mode</td><td rowspan="2">CH1 should be in sleep while CH2 and CH3 are in shutdown. VCCX should be in use.</td></tr>
<tr><td>6</td><td>54.9 kΩ</td><td>Buck</td><td>Available</td></tr>
<tr><td>7</td><td>71.5 kΩ</td><td>Boost</td><td>N/A</td><td rowspan="2">FPWM/DE Mode</td><td rowspan="2">N/A</td></tr>
<tr><td>8</td><td>90.9 kΩ</td><td>Buck</td><td>Available</td></tr>
</table>

(1) Resistor tolerance should be equal with/tighter than ±3%
(2) In FPWM mode, each channel can be dynamically and independently configurable between DE and FPWM by connecting/disconnecting 57.6 kΩ R_{SS} at the SS pin in parallel with C_{SS}.
(3) SLEEP1 should be greater than V_{SLEEP1} and SENSE1 should be greater than V_{BMIN_FIX} to open the DIS pin.

8.3.5 Fixed or Adjustable Output Regulation Target (VOUT, FB)

The output regulation targets are also selected during the initial configuration. If a channel is configured as a buck, the output regulation target can be programmed to a fixed 3.3-V output by connecting FB to AGND with a maximum resistance of 2.0 kΩ, or a fixed 5.0-V output by connecting FB to VDD with a maximum resistance of 2.0 kΩ. By connecting external feedback resistors whose parallel resistance is greater than 4.0 kΩ (see Equation 2), the output regulation target can be adjusted during operation.

$$4\ k\Omega < \frac{R_{FBT} \times R_{FBB}}{R_{FBT} + R_{FBB}} \tag{2}$$

If CH2 and CH3 are configured as a dual-phase buck, they will operate together as a dual-phase interleaved buck and the common output voltage is programmed by FB2.

If CH1 is configured as a boost, the channel requires external feedback resistors to set the output regulation target.

The internal error amplifier reference is 0.8 V. To adjust the output regulation target, select the feedback resistor values as follows.

$$V_{LOAD} = 0.8 \times \left(\frac{R_{FBT}}{R_{FBB}} + 1 \right) \tag{3}$$

The recommended minimum value for R_{FBT} is 10 kΩ.

Table 8-2. Output Regulation Targets

<table>
<tr><th rowspan="2">FB SELECTION</th><th colspan="4">SINGLE-PHASE</th><th>DUAL-PHASE</th></tr>
<tr><th>CH1 : BOOST</th><th>CH1 : BUCK</th><th>CH2 : BUCK</th><th>CH3 : BUCK</th><th>CH2//CH3 : BUCK(1)</th></tr>
<tr><td>FB = VDD</td><td>N/A</td><td colspan="4">5.0 V(2)</td></tr>
<tr><td>FB = AGND</td><td>N/A</td><td colspan="4">3.3 V(2)</td></tr>
<tr><td>FB = FB resistors</td><td colspan="5">ADJ. (VOUT range : 0.8 - 42 V)</td></tr>
</table>

(1) In dual-phase configuration, the output voltage is programmed by FB2.
(2) If other fixed output regulation targets are required, please contact the sales office/distributors for availability.

To reset and reconfigure the device, all the EN pins and the VCC_HOLD pin should be less than V_{EN} and V_{SYNC}, respectively, or VCC must be fully discharged. The preferred way to reconfigure the device is to toggle all three EN and VCC_HOLD pins together.

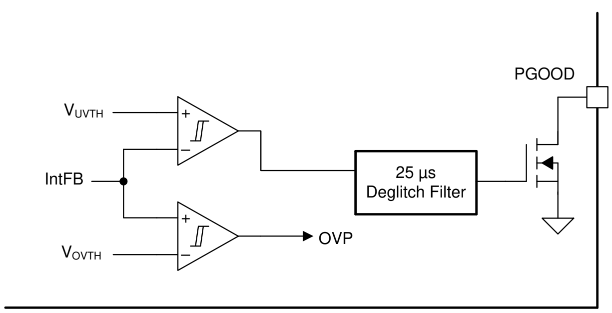
8.3.6 Overvoltage Protection (VOUT, FB)

The device provides the output overvoltage protection (OVP). The OVP comparator monitors an internal FB node which is connected to either the VOUT pin through internal FB resistors or the external FB pin. OVP is triggered when the voltage at the internal FB node or the external FB pin rises above the overvoltage threshold (V_{OVTH}). In buck configuration, the high-side driver turns off during OVP, and the low-side driver turns on until zero current is detected if the light load switching mode is either DE or skip mode. In FPWM, the device turns on the low-side driver by force until the high-side switch turns on again.

When FB is greater than V_{OVTH} for 16 consecutive clock cycles in boost, the low-side driver turns off and the high-side driver turns on 100% by force. Especially when FB is greater than V_{OVTH} in boost skip mode, the low-side driver turns off immediately and the high-side driver turns on until zero current is detected.

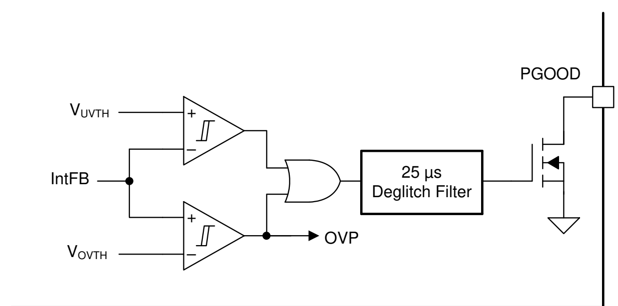
8.3.7 Power Good Indicator (PGOOD)

The device provides a dedicated power-good indicator (PGOOD) per channel to simplify sequencing and supervision. PGOOD is an open-drain output and a pullup resistor between 5 kΩ and 100 kΩ can be externally connected. In boost configuration, the PGOOD switch opens when the internal FB is greater than the undervoltage threshold (V_{UVTH}). In buck configuration, the PGOOD switch opens when the internal FB is greater than the FB undervoltage threshold and is less than the FB overvoltage threshold. The PGOOD pin is pulled down to ground if EN is less than V_{EN} and requires the VCC pin voltage to be greater than $V_{VCC\text{-}UVLO}$ to work. PGOOD3 is disabled in dual-phase buck configuration. And also FB3 should be grounded in dual-phase buck configuration.



(a)

Figure 8-5. Power Good Monitor (a) Boost configuration



(b)

Figure 8-6. Power Good Monitor (b) Buck configuration

8.3.8 Programmable Switching Frequency (RT)

The switching frequency is set by a single RT resistor connected between RT and AGND if no external synchronization clock is applied to SYNC. The resistor value to set the RT switching frequency is in Equation 4.

$$R_T = \frac{2.21 \times 10^{10}}{f_{RT(TYPICAL)}} - 955 \quad (4)$$

The RT pin is regulated to 0.5 V by an internal RT regulator when the device is in active mode or during initial configuration. CH1 clock is in phase with CH3. CH2 and CH3 are 180° out of phase. The switching frequency can be dynamically programmed during operation as shown in Figure 8-7.

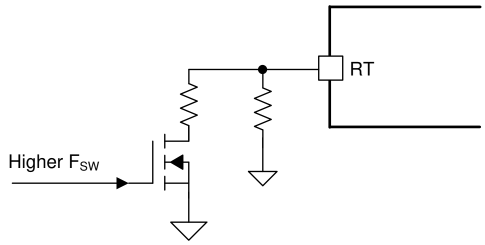


Figure 8-7. Frequency Hopping Example

8.3.9 External Clock Synchronization (SYNC)

The switching frequency can be synchronized to an external clock by directly applying an external pulse signal to SYNC. The internal CH1 and CH3 clocks are synchronized at the rising edge of the external synchronization pulse. The internal clocks of CH2 is 180° phase-shifted from CH3 clock using an internal PLL. Connect SYNC to ground if not used.

The external synchronization pulse must be greater than $V_{SYNC\text{-}RISING}$ in high logic state and must be less than $V_{SYNC\text{-}FALLING}$ in low logic state. The duty cycle of the external synchronization pulse is not limited, but the minimum on-pulse and the minimum off-pulse widths should be greater than 100 ns. The frequency of the external synchronization pulse should satisfy the following two inequalities.

$$200kHz \le f_{SYNC} \le 2.2MHz \quad (5)$$

$$0.75 \times f_{RT(typical)} \le f_{SYNC} \le 1.5 \times f_{RT(typical)} \quad (6)$$

For example, RT resistor is required for 350-kHz switching to cover from 263-kHz to 525-kHz clock synchronization without changing the RT resistor value.

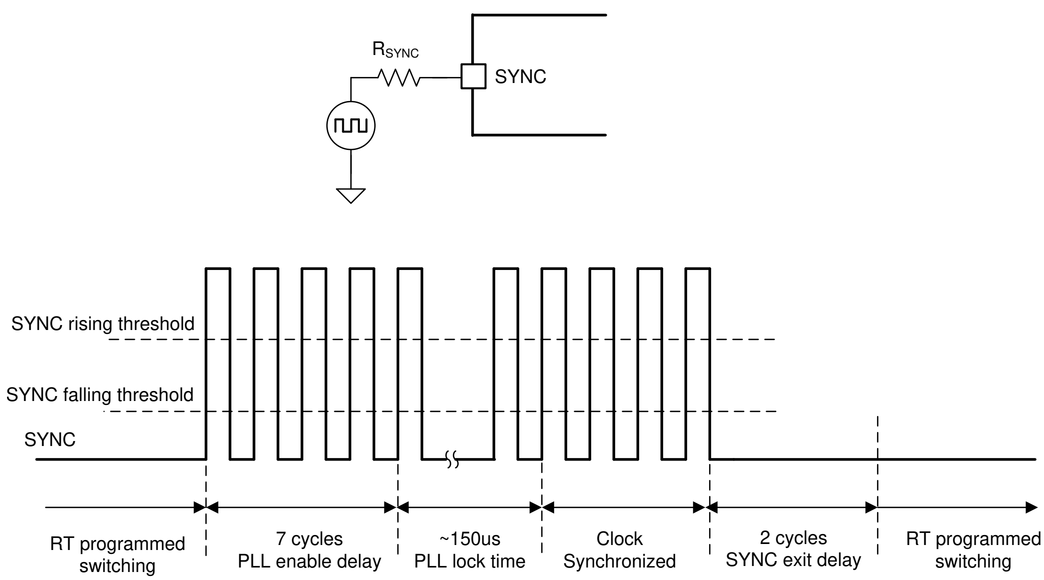


Figure 8-8. External Clock Synchronization

Drive the SYNC pin through minimum 1-kΩ resistor if the BIAS pin voltage is less than the SYNC pin voltage in any conditions.

8.3.10 Programmable Spread Spectrum (DITHER)

The device provides an optional spread spectrum (clock dithering) function that is enabled by connecting a capacitor between DITHER and AGND. A triangular waveform centered at 1.0 V is generated across the dither capacitor. This triangular waveform modulates the oscillator frequency by ±7% of the frequency set by the RT resistor. The dither capacitance value sets the rate of the low frequency modulation. For the dithering circuit to effectively reduce peak EMI, the modulation rate must be much less than the RT switching frequency. The dither capacitance which is required for a given the modulation frequency (f_{MOD}) can be calculated from following equation. Setting the f_{MOD} to 9 kHz or 10 kHz is a good starting point.

$$C_{DITHER} = \frac{20\mu A}{f_{MOD} \times 0.29} \quad (7)$$

Connecting DITHER to AGND disables clock dithering, and the internal oscillator operates at a fixed frequency set by the RT resistor. Clock dithering is also disabled when an external synchronization pulse is applied.

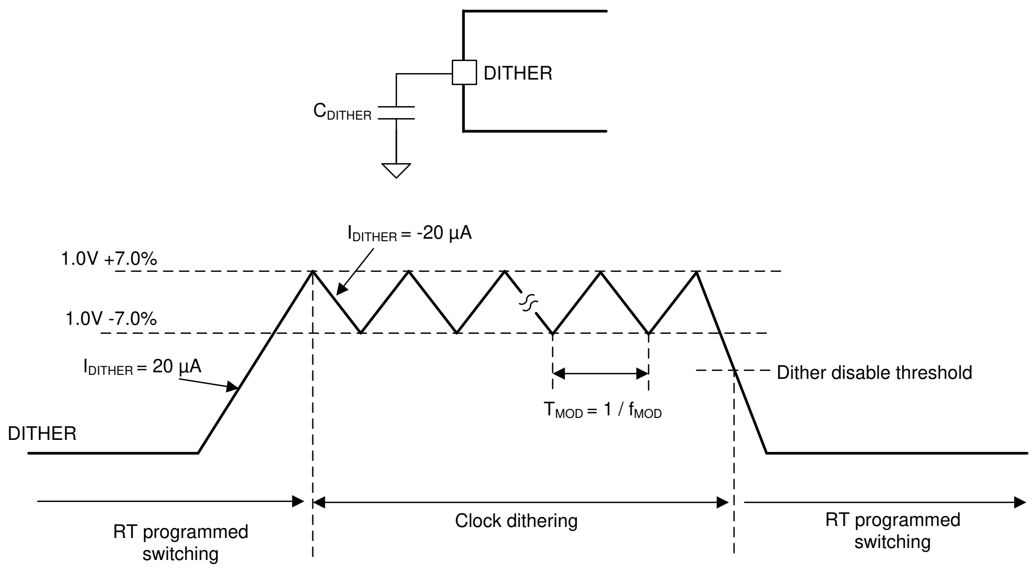


Figure 8-9. Switching Frequency Dithering

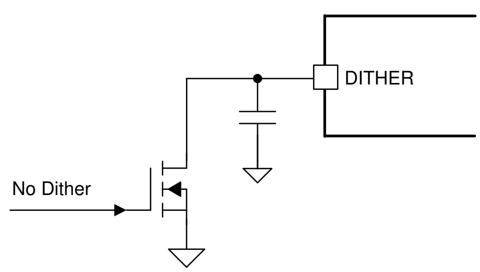


Figure 8-10. Dynamic Dither On/Off Example

8.3.11 Programmable Soft Start (SS)

The soft-start feature helps the converter gradually reach the steady state operating point. To reduce start-up stresses and surges, the device regulates the error amplifier reference to the SS pin voltage or the internal 0.8-V reference, whichever is lower.

The internal 20-µA soft-start (I_{SS1}) current turns on 130 µs after the VCC pin voltage crosses over $V_{VCC\text{-}UVLO}$. I_{SS1} gradually increases the voltage on an external soft-start capacitor (C_{SS}). This results in a gradual rise of the output voltage.

In FPWM mode, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin voltage is greater than 1.5 V, the external soft-start capacitor is charged by a 2-µA soft-start current (I_{SS2}) and the device gradually changes the zero current detection threshold (V_{ZCD}) to achieve smooth transition from the forced diode emulation to FPWM.

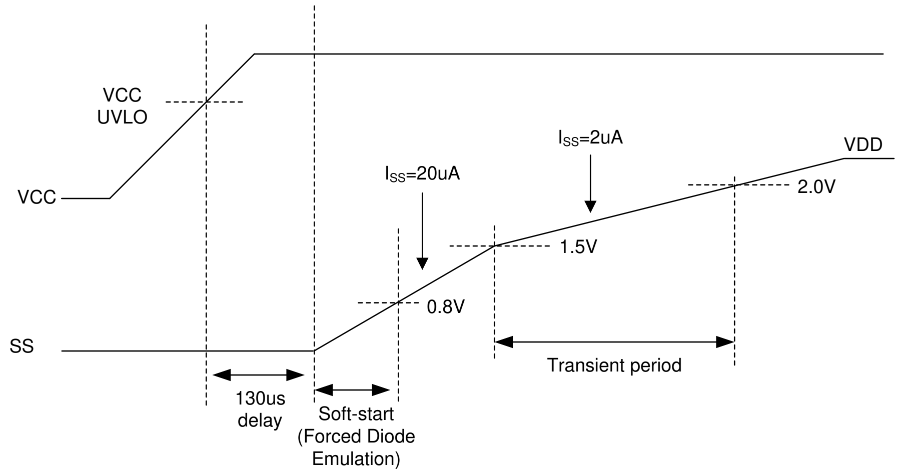


Figure 8-11. Soft-start and Smooth Transition to FPWM

In buck or SEPIC topologies, the soft-start time (t_{SS}) is calculated in Equation 8.

$$t_{SS} = 0.8 \times \frac{C_{SS}}{20\mu A} \quad (8)$$

In boost topology, t_{SS} varies with the input supply voltage because the boost output voltage is equal to the boost input voltage at the beginning of the soft-start switching. t_{SS} in boost topology is calculated in Equation 9.

$$t_{SS} = 0.8 \times \frac{C_{SS}}{20\mu A} \times \left(1 - \frac{V_{SUPPLY}}{V_{LOAD}}\right) \quad (9)$$

In general, it is recommended to choose a soft-start time long enough so that the converter can start up without going into an overcurrent state.

The device also features an internal 80-mV FB-to-SS clamp which is enabled after eight cycles with current limit. This clamp helps to minimize start-up surges after output shorts or overload situations.

8.3.12 Fast Re-start using VCC_HOLD (VCC_HOLD)

If all EN pins are less than V_{EN} and VCC_HOLD is greater than V_{SYNC} after the initial configuration is finished, the device shuts down all three channels, but keeps VCC and VDD active to restart quickly without the initial configuration delay. If CH1 is configured as a buck, the battery monitor is also enabled in this mode.

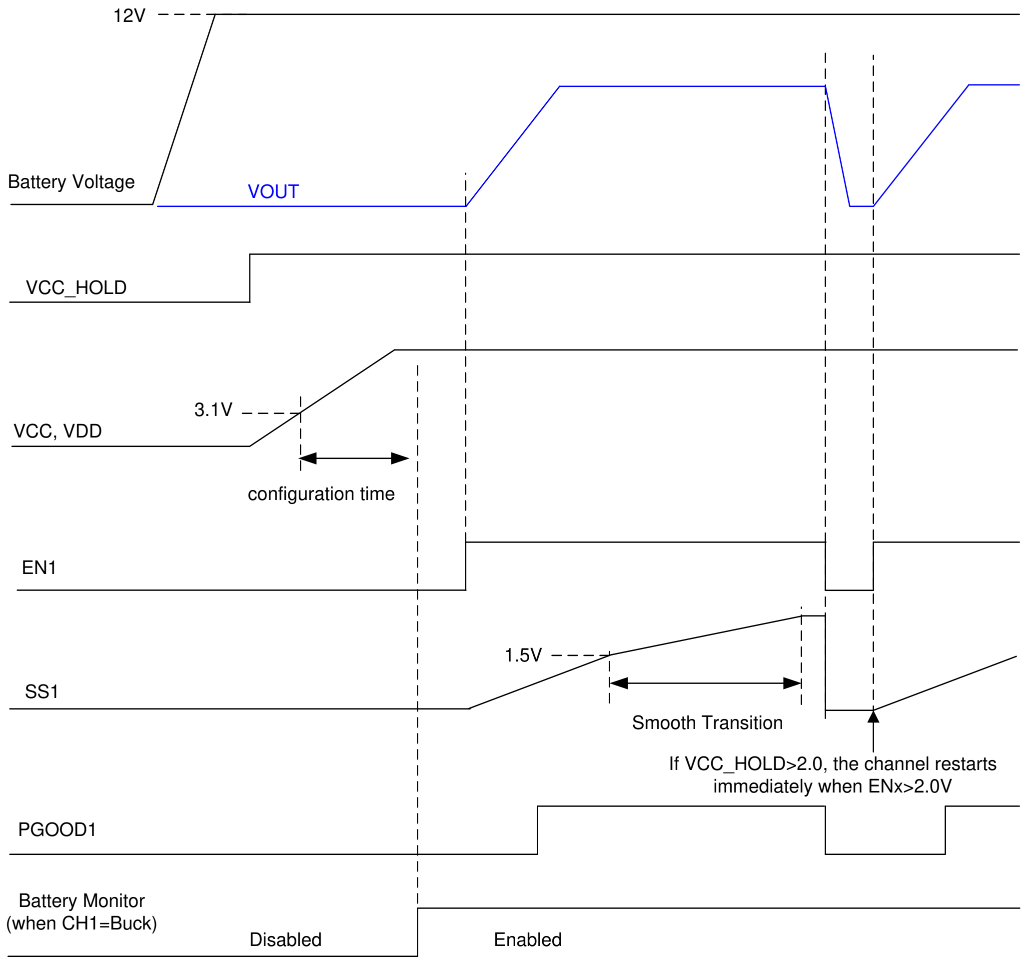


Figure 8-12. Start-up Sequence (VCC_HOLD > 2.0 V, CH1 = Buck)

8.3.13 Transconductance Error Amplifier and PWM (COMP)

The internal (or external) feedback resistor voltage divider is connected to an internal transconductance error amplifier which features high output resistance (R_O = 10 MΩ) and wide bandwidth (BW = 3 MHz). The internal transconductance error amplifier sinks (or sources) current which is proportional to the difference between the FB pin (or internal FB node) and the error amplifier reference.

The output of the error amplifier is connected to the COMP pin, allowing the use of a Type-2 loop compensation network. R_{COMP}, C_{COMP}, and optional C_{HF} loop compensation components configure the error amplifier gain and phase characteristics to achieve a stable loop response. This compensation network creates a pole at very low frequency, a mid-band zero, and a high frequency pole.

The PWM comparator in Figure 8-13 compares the sum of sensed inductor current, slope compensation ramp and a 0.3-V internal CS-to-PWM offset (V_{OFFSET}) with the COMP pin voltage, and terminates the present cycle if the sum is greater than the COMP pin voltage.

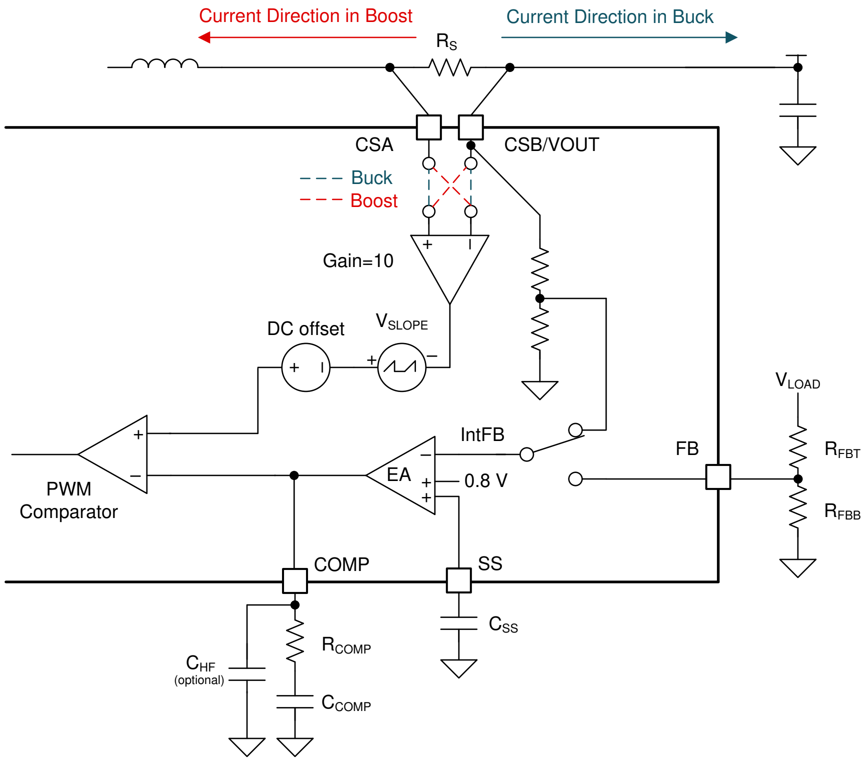


Figure 8-13. Error Amplifier, Current Sense Amplifier, and PWM

8.3.14 Current Sensing and Slope Compensation (CSA, CSB)

The device features high-side current sense amplifiers with an effective gain of 10 (A_{CS}), and provides an internal slope compensation ramp to the PWM comparator to prevent a subharmonic oscillation at high duty cycle. The device generates the 0.8 V-peak (at 100% duty cycle) slope compensation ramp at the PWM comparator input.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than at least half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle. Therefore, the minimum amount of the slope compensation should satisfy the following inequality.

$$0.5 \times \frac{V_{LOAD}}{L_M} \times R_S \times 10 \times Margin < 0.8 \times f_{SW} \; (Buck) \tag{10}$$

$$0.5 \times \frac{V_{LOAD} - V_{SUPPLY}}{L_M} \times R_S \times 10 \times Margin < 0.8 \times f_{SW} \; (Boost) \tag{11}$$

where

- 1.5-1.7 is recommended as the margin to cover non-ideal factors.

8.3.15 Constant Peak Current Limit (CSA, CSB)

In boost configuration, if the current sense amplifier input exceeds the 60-mV cycle-by-cycle current limit threshold (V_{CLTH}), the current limit comparator immediately terminates LO and turns on HO. In buck configuration, if the current sense amplifier input exceeds V_{CLTH}, the current limit comparator immediately terminates HO and turns on LO.

The device provides a constant peak current limit whose peak inductor current limit is constant over the input and output voltage. For the case where the inductor current may overshoot, such as inductor saturation, the current limit comparator skips pulses until the current has decayed below the current limit threshold.

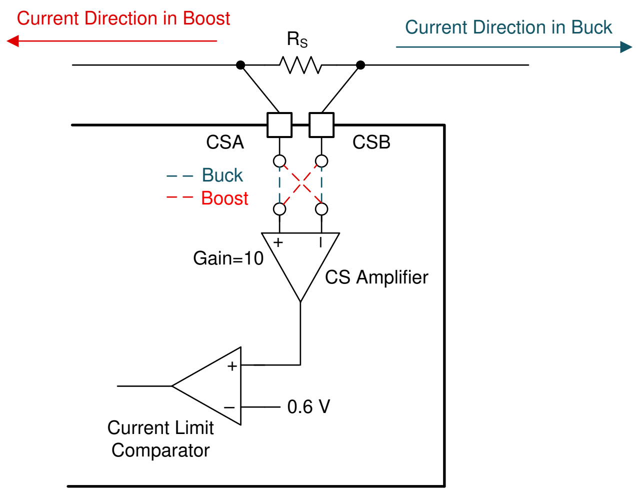


Figure 8-14. Current Limit Comparator

Cycle-by-cycle peak current limit is calculated as follows:

$$I_{PEAK-CL} = \frac{0.06}{R_S} \tag{12}$$

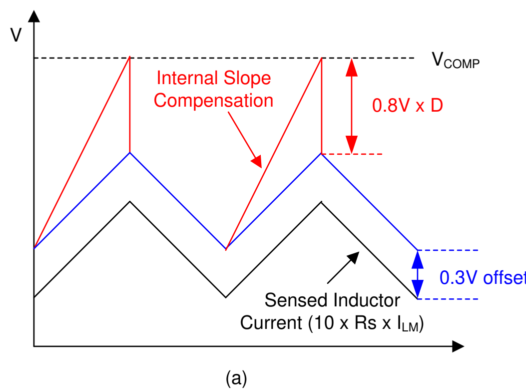


Figure 8-15. (a) PWM Comparator Input

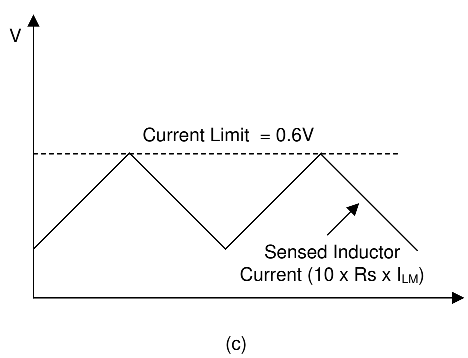


Figure 8-16. (b) Current Limit Comparator Input (Buck and Boost)

Boost converters have a natural pass-through path from the supply to the load through the high-side MOSFET body diode. Due to the pass-through path and the limitation of the minimum controllable on-time, boost converters cannot provide current limit protection when the output voltage is close to or less than the input supply voltage.

8.3.16 Maximum Duty Cycle and Minimum Controllable On-time Limits (Boost)

In boost configuration, the device limits the maximum duty cycle of the low-side driver. This maximum duty cycle limit ($D_{MAX\text{-}BOOST}$) decides the minimum input supply voltage which can achieve the target output voltage during CCM operation. The minimum input supply voltage ($V_{SUPPLY(MIN)}$) which can achieve the target output voltage is not limited by $D_{MAX\text{-}BOOST}$ during DCM operation. The minimum input supply voltage which can achieve the target output voltage in CCM can be estimated using Equation 13.

$$V_{SUPPLY(MIN)} \approx V_{LOAD} \times (1 - D_{MAX-BOOST}) + I_{SUPPLY(MAX)} \times (R_{DCR} + R_S + R_{DS(ON)}) \quad (13)$$

At light load conditions or when the input voltage is close to the target output voltage in CCM, the device skips the low-side driver pulses if the required on-time is less than the boost minimum controllable on-time ($t_{ON\text{-}MIN\text{-}BOOST}$). This pulse skipping appears as a random behavior.

If the input voltage is further increased to the voltage higher than the target output voltage, the required-on-time becomes zero and eventually the device enters a bypass mode which turns on the high-side driver 100% when V_{FB} is greater than V_{OVTH}.

8.3.17 Bypass Mode (Boost)

In boost configuration when the boost channel is used as a pre-boost, bypass mode operation is useful to reduce the losses of the high-side MOSFET when the converter input voltage is higher than the converter output regulation target. The device supports bypass mode operation by using an internal charge pump which is enabled in active mode. Because the internal charge pump generates V_{BIAS} + 5 V to supply HB1, the BIAS pin should be connected to the output or input of the boost converter to supply enough voltage to HB1 when the converter input voltage is higher than the converter output regulation target.

During CCM operation or when the device is configured in FPWM mode, the high-side driver naturally turns on 100% without any replenish switching when the required on-time becomes less than zero and the input voltage is greater than the target output voltage. If the input supply voltage satisfies the following inequality in CCM, the boost channel starts random pulse skipping and eventually enters bypass mode.

$$V_{SUPPLY(PulseSkip)} > V_{LOAD} \times (1 - f_{SW} \times t_{ON-MIN-BOOST}) + I_{SUPPLY} \times (R_{DCR} + R_S + R_{DS(ON)}) \quad (14)$$

Table 8-3. Typical Boost Input Supply Voltage to Start Pulse Skipping in CCM

	7-V OUTPUT	8.5-V OUTPUT
f_{SW} = 440 kHz	> 6.8 - 6.9 V	> 8.2 - 8.3 V
f_{SW} = 2.2 MHz	> 5.9 - 6.0 V	> 7.2 - 7.3 V

During DCM operation, the device enters the bypass mode 16 cycles after the FB1 pin voltage is greater than V_{OVTH}. In this bypass mode, the device turns on the high-side driver 100% by force.

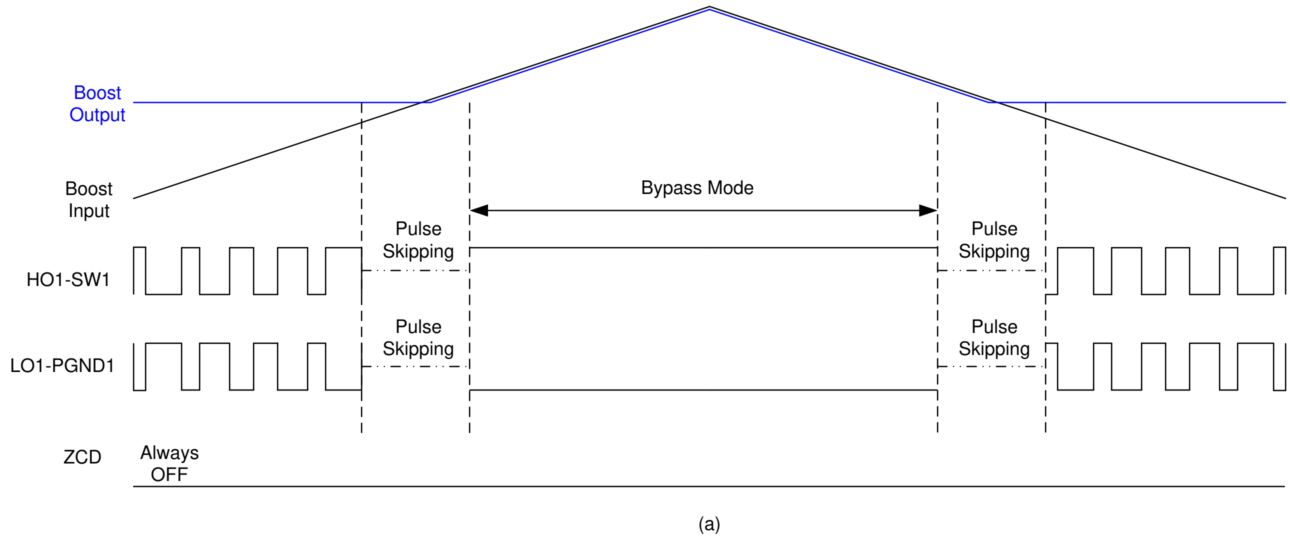


Figure 8-17. PWM to Bypass Mode Transition (a) During CCM

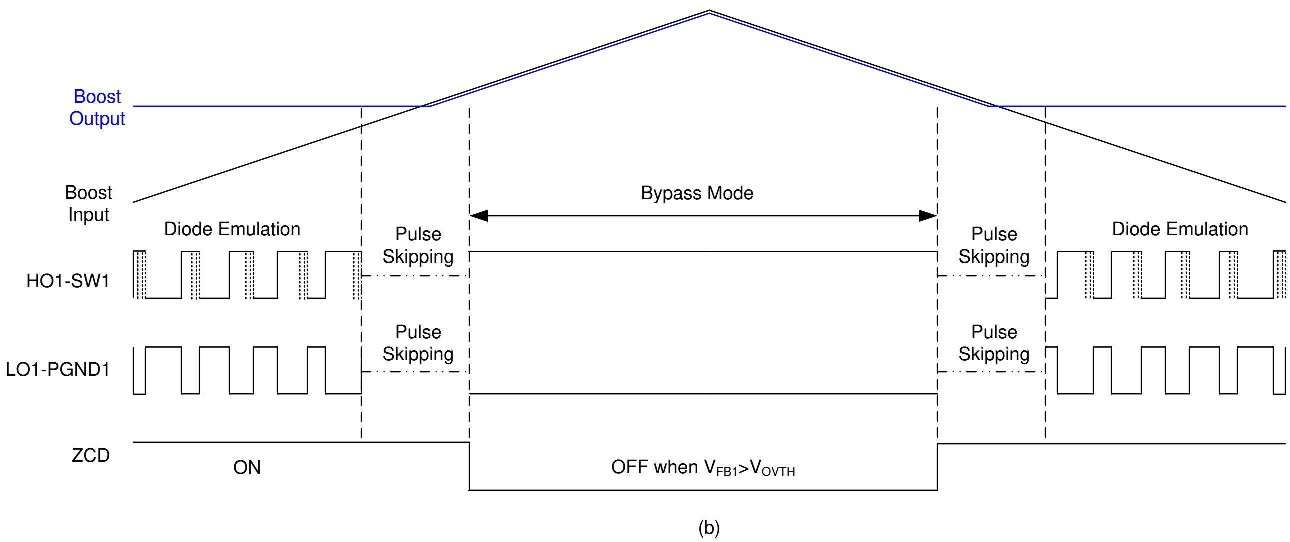


Figure 8-18. PWM to Bypass Mode Transition (b) During DCM

Table 8-4. Switching Operation in Boost Configuration

CONDITION	LIGHT LOAD SWITCHING MODE		
	SKIP MODE	DIODE EMULATION (USE R_{SS} IN FPWM)	FPWM MODE
$V_{SUPPLY} > V_{LOAD}$	Enters bypass mode (HO turns on 100%) when FB1 > V_{OVTH}. During CCM, HO turns on 100% if the required on-time is zero.		
$V_{SUPPLY} \approx V_{LOAD}$ or at light load condition	Once LO driver turns on, the device keeps the LO driver on until the minimum peak current limit is satisfied. Random pulse skipping happens when the required peak current is less than the minimum peak current.	Random pulse skipping happens when the required on-time is less than the minimum on-time.	
$V_{SUPPLY} < V_{LOAD}$	PWM operation with diode emulation		PWM operation in FPWM mode
$V_{SUPPLY} << V_{LOAD}$	Out-of-regulation when the required duty cycle is greater than the maximum duty cycle limit		

8.3.18 Minimum Controllable On-time and Minimum Controllable Off-time Limits (Buck)

In buck configuration, the device starts pulse skipping at the light load condition or when the input voltage is much higher than the target output voltage in CCM. The device skips the high-side driver pulses if the required on-time is less than the buck minimum controllable on-time ($t_{ON\text{-}MIN\text{-}BUCK}$). This pulse skipping appears as a random behavior.

If the input supply voltage satisfies the following inequality in CCM, the buck channel starts random pulse skipping.

$$V_{SUPPLY(PulseSkip)} > \frac{V_{LOAD} + I_{LOAD}\left(R_{DCR} + R_S + R_{DS(ON)}\right)}{t_{ON-MIN-BUCK} \times f_{SW}} \quad (15)$$

Table 8-5. Typical Buck Input Supply Voltage to Start Pulse Skipping in CCM

	3.3-V OUTPUT	5.0-V OUTPUT
f_{SW} = 440 kHz	No pulse skipping in CCM	No pulse skipping in CCM
f_{SW} = 2.2 MHz	> 20 - 23 V	> 31 - 34 V

In buck configuration, the maximum duty cycle of the high-side driver is limited by the buck minimum controllable off-time ($t_{OFF\text{-}MIN\text{-}BUCK}$). $t_{OFF\text{-}MIN\text{-}BUCK}$ decides the minimum input supply voltage that can achieve the target output voltage in normal PWM operation. If the input voltage falls down below this minimum input supply voltage in normal PWM operation, the device enters a low-dropout (LDO) mode to extend the minimum input voltage further down. If the input supply voltage satisfies the following inequality, the buck channel enters a low drop-out mode.

$$V_{SUPPLY(LDO)} < \frac{V_{LOAD} + I_{LOAD}\left(R_{DCR} + R_S + R_{DS(ON)}\right)}{1 - t_{OFF-MIN-BUCK} \times f_{SW}} \quad (16)$$

Table 8-6. Typical Buck Input Supply Voltage to Enter LDO Mode

	3.3-V OUTPUT	5.0-V OUTPUT
f_{SW} = 440 kHz	< 3.6 - 3.8 V	< 5.5 - 5.6 V
f_{SW} = 2.2 MHz	< 4.3 - 4.5 V	< 6.6 - 6.7 V

8.3.19 Low Dropout Mode for Extended Minimum Input Voltage (Buck)

When the soft start is finished, the buck channel can enter the LDO mode if the required duty cycle is greater than the maximum duty cycle which is limited by $t_{OFF\text{-}MIN\text{-}BUCK}$. During the LDO mode, the buck channels individually extends its on-time pulse to the next cycle until the PWM comparator trips. The buck channel turns off the high-side driver for 110 ns by force when the replenish pulse counter detects 15 cycles of consecutive low-side driver pulse skipping. The minimum input supply voltage which can achieve the target output voltage during the LDO mode is estimated from the following equation.

$$V_{SUPPLY(MIN)} \approx \frac{V_{LOAD} + I_{LOAD(MAX)} \times \left(R_{DCR} + R_S + R_{DS(ON)}\right)}{1 - \frac{t_{OFF-MIN-BUCK}}{16} \times f_{SW}} \quad (17)$$

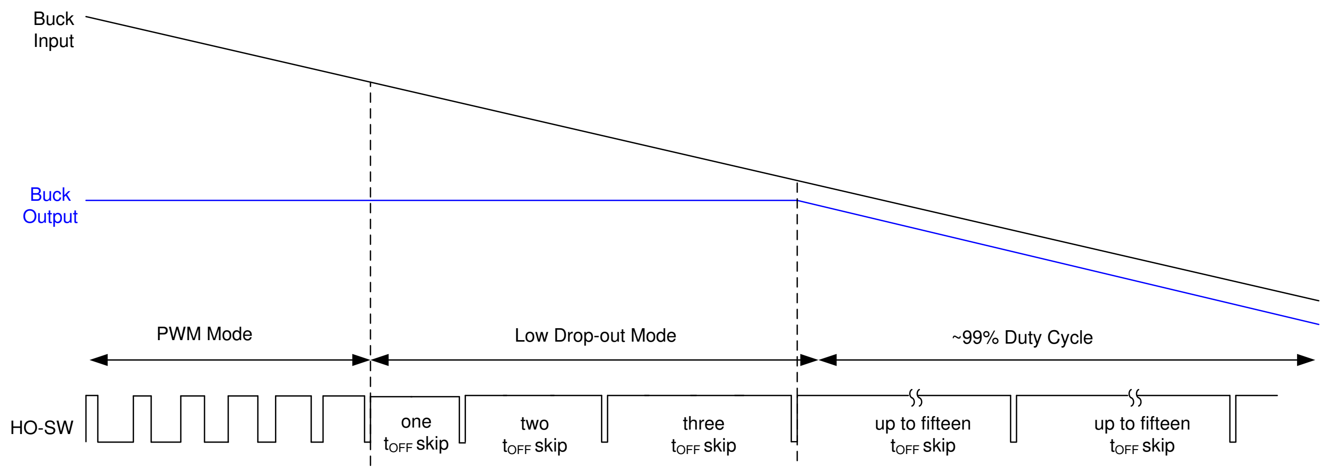


Figure 8-19. PWM to LDO Mode Transition

Table 8-7. Switching Operation in Buck Configuration

CONDITION	LIGHT LOAD SWITCHING MODE		
	SKIP MODE	DIODE EMULATION (USE R_{SS} IN FPWM)	FPWM MODE
V_{SUPPLY} >> V_{LOAD} or at light load condition	Once HO driver turns on, the device keeps the HO driver on until the minimum peak current limit is satisfied. Random pulse skipping happens when the required peak current is less than the minimum peak current.	Random pulse skipping happens when the required on-time is less than the minimum on-time.	
V_{SUPPLY} > V_{LOAD}	PWM operation with diode emulation		PWM operation in FPWM mode
$V_{SUPPLY} \approx V_{LOAD}$	Enters LDO mode when the required duty cycle is greater than the maximum duty cycle limit which is defined by $t_{OFF-MIN-BUCK}$.		
V_{SUPPLY} < V_{LOAD}	Out of regulation when the required duty cycle is greater than approximately 99%		

8.3.20 Programmable Hiccup Mode Overload Protection (RES)

The device includes programmable hiccup mode overload protection which is enabled when a capacitor (C_{RES}) is connected to the RES pin in buck configuration. The hiccup mode overload protection is disabled in boost configuration or RES is connected to VDD during initial power-on.

In normal operation, C_{RES} is discharged to ground and an internal fault counter counts the clocks when cycle-by-cycle current limiting occurs. When the fault counter detects 256 cycles of switching with current limit on any buck channel, an internal hiccup mode off-timer forces the applicable channel to stop switching and starts sourcing 20 µA of current (I_{RES}) into C_{RES}. During this hiccup mode overload protection, the off-time before the channel restart (T_{RES}) is programmed by C_{RES}. During T_{RES}, the HO and the LO outputs are disabled and C_{SS} is charged by I_{RES}. When the RES pin voltage reaches the RES threshold (V_{RESTH}) , C_{RES} is discharged by an internal RES pull-down switch, and C_{SS} begins to charge with 30us delay. The 256 cycle fault counter is reset if eight consecutive switching cycles occur without current limit.

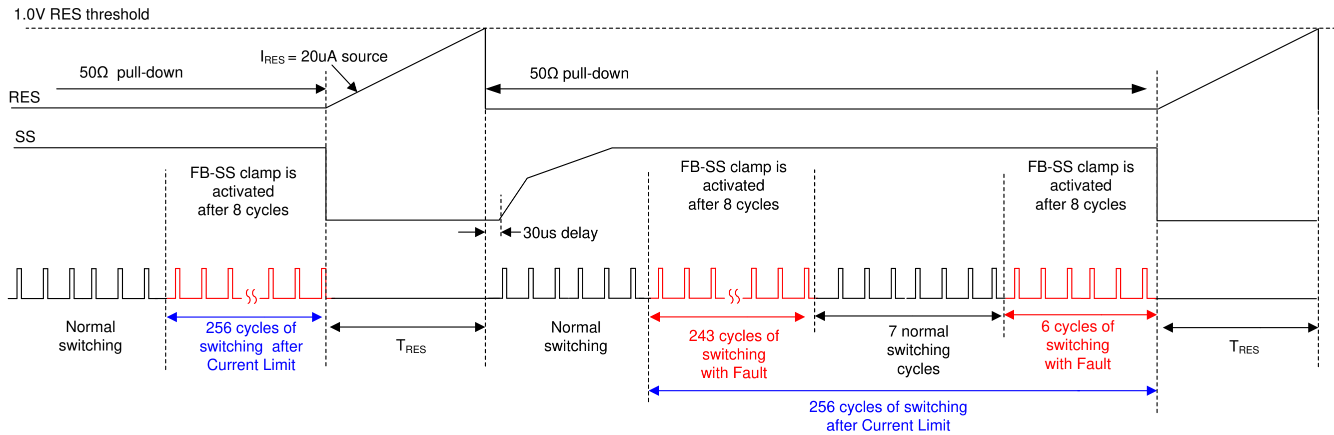


Figure 8-20. Hiccup Mode Overload Protection (Single Channel Fault)

The device provides an independent fault counter per channel, but the RES pin is shared by all channels. The device allows that one channel is in the hiccup mode off while the other channels operate normally. In the event that multiple channels are in a fault condition, the last fault counter pulls the RES pin low and starts the RES capacitor charging cycle. Then, the multiple channels which are in the fault condition restart together when the RES pin voltage reaches V_{RESTH}. If CH2 and CH3 are configured as an interleaved dual-phase buck, the fault counters count the fault independently, but both CH2 and CH3 stop switching and restart together.

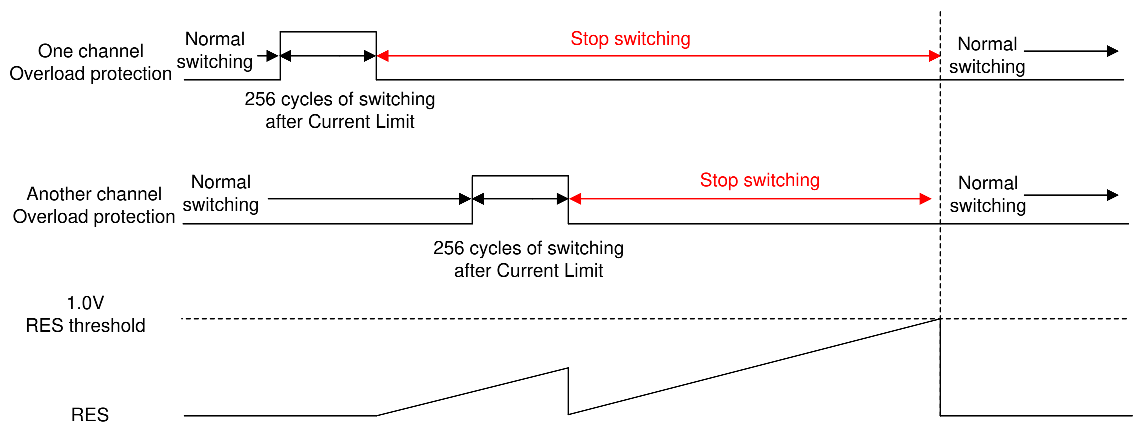


Figure 8-21. Hiccup Mode Overload Protection (Multiple Channel Faults)

The hiccup mode protection is also programmed during the initial configuration time. If RES is connected to VDD during the initial configuration time, the internal fault counter is disabled and the device operates with non-hiccup mode cycle-by-cycle current limit. If RES is connected to AGND, the applicable channel that detects 256 cycles of current limiting stops switching and then never restarts until the applicable channel's EN pin is toggled.

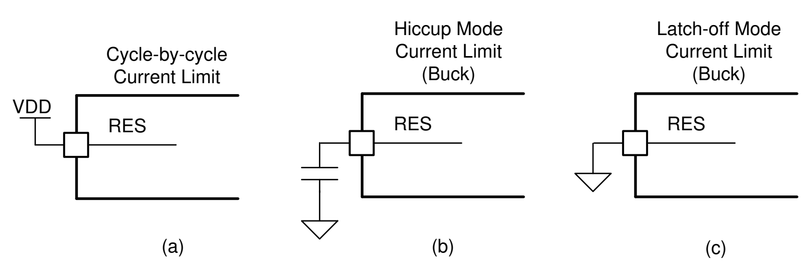


Figure 8-22. Hiccup Mode Configuration

Table 8-8. Overload Protection Configurations

RES SELECTION	SINGLE-PHASE				DUAL-PHASE
	CH1 : BOOST	CH1 : BUCK	CH2 : BUCK	CH3 : BUCK	CH2//CH3 : BUCK
RES = VDD	Cycle-by-cycle current limit	Cycle-by-cycle current limit			
RES = C_{RES}		Hiccup mode current limit			
RES = AGND		Latch-off mode current limit			

8.3.21 MOSFET Drivers and Hiccup Mode Fault Protection (LO, HO, HB)

The device provides N-channel logic MOSFET drivers which can source a peak current of 2.2 A and sink a peak current of 3.3 A. The drivers are powered by VCC or HB, and enabled when EN is greater than V_{EN} and VCC is greater than $V_{VCC\text{-}UVLO}$.

When the low-side driver turns on, the SW pin voltage is approximately 0 V and the C_{HB} is charged from VCC through a boot diode. In boost configuration, the boot diode is internally connected from VCC to HB1. Connect external boot diodes in buck configuration. The recommended minimum value of C_{HB} is 0.1-μF.

The LO and HO outputs are controlled with an adaptive dead-time methodology which ensures that both outputs are not enabled at the same time. When the device commands LO to be enabled, the adaptive dead-time logic first disables HO and waits for HO-SW voltage to drop. LO is then enabled after a small delay. Similarly, the HO turnon is delayed until the LO-PGND voltage has discharged. HO is then enabled after a small delay. The adaptive dead-time circuit insures that both outputs are not enabled at the same time when $Q_{G@5V}$ is less than 40 nC over the temperature.

If the minimum BIAS pin voltage is below $V_{VCC\text{-}REG}$, extra care should be taken when selecting the MOSFETs. Especially during start-up at low BIAS input voltage, the gate plateau voltage of the MOSFET should be less than the BIAS pin voltage to completely enhance the MOSFET. If the driver output voltage is lower than the MOSFET gate plateau voltage during start-up, the converter may not start up properly and it can stick at the maximum duty cycle in a high power dissipation state. This condition can be avoided by selecting a lower threshold MOSFET or by turning on the channel when the BIAS pin voltage is sufficient.

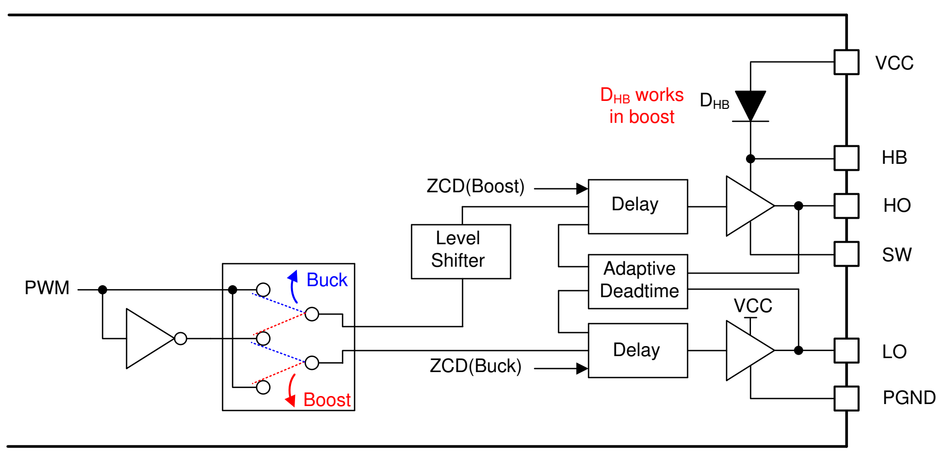


Figure 8-23. Driver Structure (Internal boot diode is available only in boost)

The hiccup mode protection is triggered by the HB UVLO in boost configuration. If the HB-to-SW voltage is less than the HB UVLO threshold ($V_{HB\text{-}UVLO}$), the LO turns on for 75 ns to replenish the boost capacitor. The device allows up to four consecutive replenish switchings. After four consecutive boot replenish switching, the channel skips the boot replenish switching for 12 cycles. If the channel fails to replenish the boost capacitor after the four sets of the four consecutive replenish switching, the channel stops switching and enters hiccup mode fault protection.

If required, the slew rate of the switching node voltage is adjusted by the resistor in series with the HB pin up to 5-Ω in buck configuration. If required, use a gate resistor in parallel with a pulldown PNP transistor. Care should be taken when adding a gate resistor as this can decrease the effective dead-time.

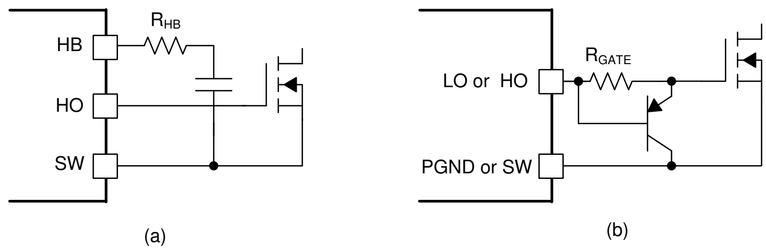


Figure 8-24. Slew Rate Control (a) HB Resistor for Buck, (b) Gate Resistor with Pulldown PNP Transistor

8.3.22 Battery Monitor (BMOUT, BMIN_FIX, BMIN_PRG)

A battery monitor function is enabled when CH1 is configured as a buck, and at least one of the EN pins is greater than V_{EN} or VCC_HOLD is greater than V_{SYNC}. If BMIN_PRG is less than BMIN_PRG threshold (V_{SLEEP}) and BMIN_FIX is greater than BMIN_FIX threshold (V_{BMIN_FIX}), BMOUT is connected to AGND. BMOUT opens when BMIN_FIX is greater than V_{BMIN_FIX} or BMIN_PRG is greater than V_{SLEEP}. By using a resistor voltage divider at BMIN_PRG, the threshold of the battery monitor can be programmed, but the resistor divider and the internal 30-µA hysteresis current (I_{SLEEP1}) will drain the battery.

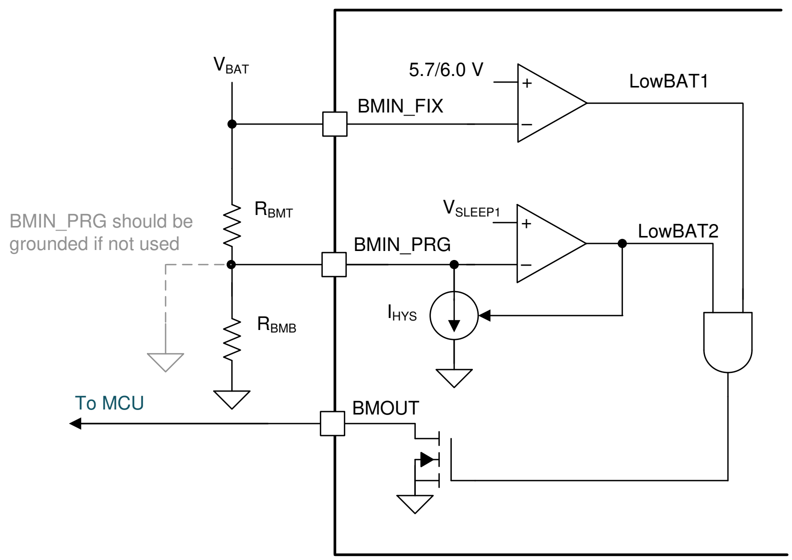


Figure 8-25. Battery Monitor

To adjust the low battery voltage detection levels, select the battery monitor resistor values as follows. The low battery falling detection level should be lower than 5.7 V and the low battery rising detection level should be higher than 6.0 V to program.

$$R_{BMT} = \frac{\left(V_{LOWBAT-RISING} - 1.022 \times V_{LOWBAT-FALLING}\right)}{30\mu A} \tag{18}$$

$$R_{BMB} = \frac{R_{BMT}}{\left(V_{LOWBAT-FALLING} - 1.0V\right)} \tag{19}$$

8.3.23 Dual-phase Interleaved Configuration for High Current Supply (CFG)

The device supports dual-phase interleaved buck configuration especially for a high current automotive processor supply. In the dual-phase configuration, COMP3 and SS3 should be left floating since the pins are internally connected to COMP2 and SS2, respectively. Also, FB3 should be grounded and PGOOD3 doesn't work. In this configuration, it is allowed to turn on CH2 while CH3 is in shutdown, but it is not allowed to turn on CH3 while CH2 is in shutdown.

In the dual-phase configuration, the EN2 pin works as a primary enable pin for both CH2 and CH3. Both CH2 and CH3 shut down when the EN2 pin is less than V_{EN}. The EN3 pin controls only the CH3 in the dual-phase configuration , which helps to add or drop just one phase.

To achieve a better inductor current balancing between two channels, it is recommended to connect both CSB1 and CSB2 at the same point on the PC board, close to the one of low-ESR output capacitors

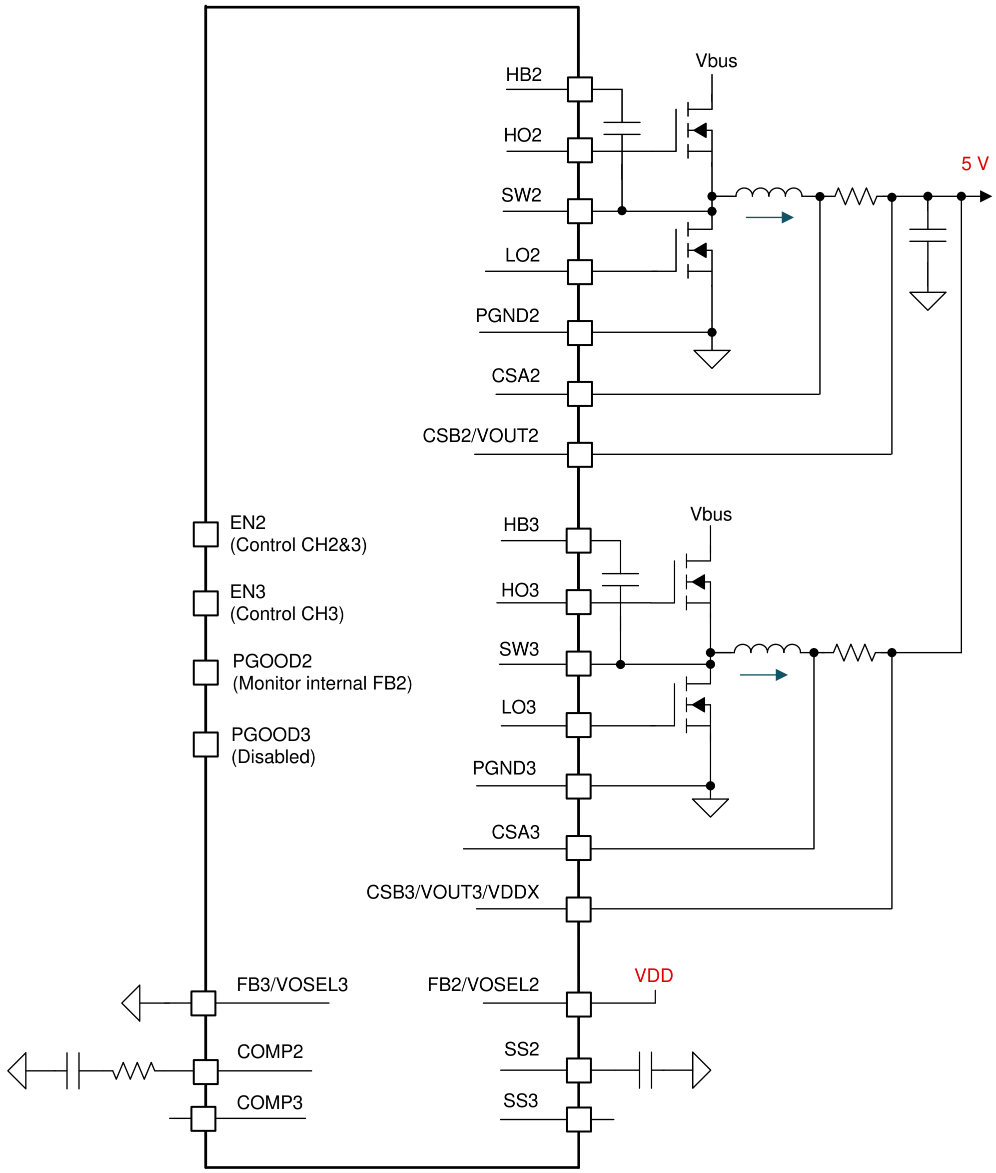


Figure 8-26. Pin Connections in Dual-phase Buck Configuration (5-V Output Example)

8.3.24 Thermal Shutdown Protection

An internal thermal shutdown is provided to protect the device in case that the junction temperature exceeds 175°C. When the thermal shutdown is activated, the device is forced into a low power thermal shutdown state with the MOSFET drivers and the VCC regulator disabled. After the junction temperature is reduced (typical hysteresis is 15°C), the device restarts.

8.3.25 External VCCX Supply Reduces Power Dissipation

The maximum power dissipation of the device is limited by the maximum ambient temperature and the power dissipation of the device. The power dissipation of the device is calculated as follows.

$$P_{IC} = V_{BIAS} \times \left(I_{BIAS} + \frac{0.5}{R_T} + 6 \times Q_{G@5V} \times f_{SW} \right) \tag{20}$$

By supplying the external VCCX supply, the power dissipation of the device can be dramatically reduced. The power dissipation of the device with 5 V VCCX is calculated as follows.

$$P_{IC} = V_{BIAS} \times I_{BIAS} + 5 \times \left(\frac{0.5}{R_T} + 6 \times Q_{G@5V} \times f_{SW} \right) \tag{21}$$

The junction temperature of the device is estimated as follows.

$$T_J = T_A + R_{\theta JA} \times P_{IC} \tag{22}$$

8.4 Device Functional Modes

8.4.1 Device Status

8.4.1.1 Shutdown Mode

When all EN pins are less than V_{EN} and VCC_HOLD pin is less than V_{SYNC}, the device shuts down with all functions disabled, consuming less than 3 µA from the BIAS pin.

8.4.1.2 Configuration Mode

During the initial power-on, when at least one of the EN pins is greater than $V_{EN,}$ or VCC_HOLD is greater than V_{SYNC}, the device programs the light load switching mode, the output regulation target, the device configuration and the hiccup mode protection. To reset and reconfigure the device, all the EN pins and the VCC_HOLD pin should be less than V_{EN} and V_{SYNC}, respectively, or VCC must be fully discharged. The preferred way to reconfigure the device is to toggle all three EN and VCC_HOLD pins together.

8.4.1.3 Active Mode

After the initial configuration is finished, the device enters active mode with all functions enabled. In this active mode, the HB1 charge pump is enabled to support bypass mode operation if the CH1 is configured as a boost.

8.4.1.4 Sleep Mode

When the device is configured as a skip mode, the buck channel enters sleep mode when the high-side driver skips switching 16 consecutive cycles at light/no load conditions.

8.4.1.5 Deep Sleep Mode

The device stops internal oscillator and enters low-I_Q deep sleep mode when all enabled channels are in sleep mode, SLEEP1 is greater than V_{SLEEP1} and SENSE1 is greater than V_{BMIN_FIX}. During deep sleep mode, the DIS switch opens to cut the leakage path through the SLEEP1 resistor divider and the FB1 resistor divider if SLEEP1 is greater than V_{SLEEP1} and SENSE1 is greater than V_{BMIN_FIX}.

8.4.1.5.1 Cutting Leakage Path in Deep Sleep Mode (DIS, SLEEP1, SENSE1)

If CH1 is configured as a boost, the battery monitor function is disabled and BMIN_FIX, BMIN_PRG, and BMOUT are used as SENSE1, SLEEP1, and DIS respectively in order to minimize battery drain in the deep sleep mode. The SENSE1 pin should be connected to the drain connection of the CH1 high-side MOSFET. The SLEEP1 resistor divider can be connected to the battery or the output of the boost converter through a resistor divider. The SLEEP1 pin can be connected to ground if deep sleep mode is not required.

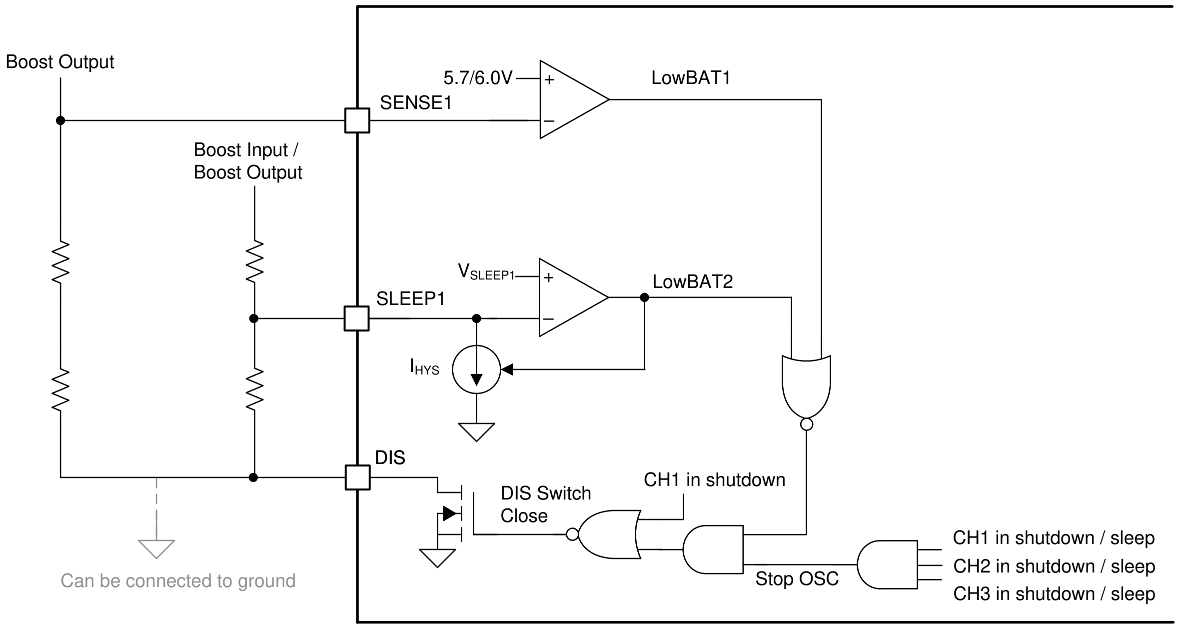


Figure 8-27. Deep Sleep when CH1 = Boost

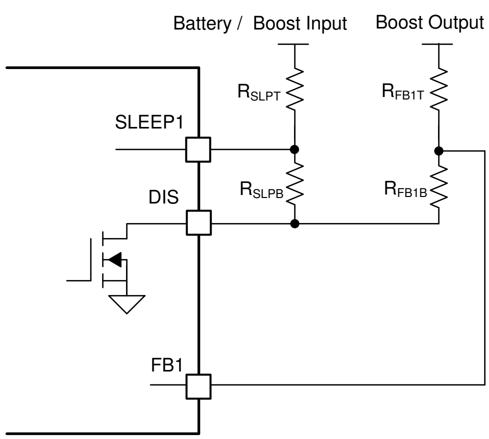


Figure 8-28. SLEEP1 Resistor Divider and FB Resistor Divider Connections

8.4.1.6 VCC HOLD Mode

After the initial configuration is finished, the device enters the VCC HOLD mode if all EN pins are less than V_{EN} and VCC_HOLD is greater than V_{SYNC}. During the VCC_HOLD mode, VCC and VDD are maintained and the battery monitor is enabled if buck configuration. The VCC_HOLD mode is useful when the device needs to restart fast without the initial configuration time delay.

Table 8-9. Pin Status in Steady State #1 (When BIAS > ~ 5.5 V)

	SHUTDOWN	CONFIGURATION	ACTIVE (CHANNEL BASE)	SLEEP (CHANNEL BASE)	DEEP SLEEP	VCC HOLD
EN	All EN pins < 0.4 V	At least one pin > 2.0 V	At least one pin > 2.0 V			All EN pins < 0.4 V
VCC_HOLD / SYNC / DITHER	< 0.4 V		SYNC/DITHER enabled		SYNC/DITHER disabled	> 2.0 V
CFG/MODE	Disabled	Enabled	Disabled			
BIAS	I_Q < 3 µA	I_Q < 150 µA	I_Q = 1.3 mA - 3.0 mA	Not specified	I_Q= ~2 µA	I_Q < 25 µA

Table 8-9. Pin Status in Steady State #1 (When BIAS > ~ 5.5 V) (continued)

	SHUTDOWN	CONFIGURATION	ACTIVE (CHANNEL BASE)	SLEEP (CHANNEL BASE)	DEEP SLEEP	VCC HOLD
VCC	Discharged	VCC regulator is enabled	VCC regulator is enabled if VCCX is not in use.		Active with 1-mA current limit if VCCX is not in use.	
VCC-VCCX switch	Open with diode path		Closed if VCCX > 4.4 V			
VCC-VDD switch	Open		Closed if at least one channel is active		Closed if VDDX is not in use.	Closed
VDDX-VDD switch	Open		Closed if at least one channel is active		Closed if VDDX use (VOUT3 = Fixed 3.3 V)	Open
RT	Disabled		Enabled		Disabled	
RES	Disabled	RES mode detection	Enabled if at least one channel is active		Disabled	
SENSE1 (Boost)	Disabled		Enabled			Disabled
SLEEP1 (Boost)	Disabled		Enabled		Disabled	
DIS switch (Boost)	Open		GND		Open	
BMIN_FIX (Buck)	Disabled		Active if at least one channel is active			Enabled
BMIN_PRG (Buck)	Disabled					
BMOUT switch (Buck)	Open					

Table 8-10. Pin Status in Steady State #2 (When BIAS > 5.5 V)

	SHUTDOWN	CONFIGURATION	ACTIVE (CHANNEL BASE)	SLEEP (CHANNEL BASE)	DEEP SLEEP	VCC HOLD
PGOOD (Boost)	GND (weak pull-down)	GND	Enabled, monitors UV	Monitors OV for bypass operation.	Open	GND
PGOOD (Buck)	GND (weak pull-down)	GND	Enabled, monitors both UV and OV	Open	Open	GND
FB (Boost)	Disabled	VOUT1 is adjustable.	Enabled		Disabled	
FB (Buck)	Disabled	FB mode detection	Enabled if VOUT is adjustable. Open otherwise.			Disabled
COMP (Boost)	Discharged	GND	Enabled		GND	
COMP (Buck)	Discharged	GND	Enabled. COMP3 = COMP2 if dual-phase buck			GND
SS (Boost)	Discharged	GND	Enabled	Pullup to VDD	Pullup to VDD	GND
SS (Buck)	Discharged	GND	Enabled. SS3 = SS2 if dual-phase buck	Pullup to VDD		GND
HB-SW (Boost)	Discharged	Charge pump is on	HB-SW ≈5 V	HB-SW ≈5 V by charge pump	Discharging. Charge pump is off	
HB-SW (Buck)	Discharged	Charged when VOUT<VCC	HB-SW ≈5 V	Discharging		
HO-SW (Boost)	Open	2-kΩ pulldown resistor	Switching	Pull up in bypass. Pull down otherwise	Pull up, but will be off when HB UV	Pull down
HO-SW (Buck)	Open	2-kΩ pulldown resistor	Switching	Pull down		
LO-PGND (Boost)	Open	Pull down	Switching	Pull down		
LO-PGND (Buck)	Open	Pull down	Switching	Pull down		

8.4.2 Light Load Switching Mode

The light load switching mode of the device is programmed to either the forced PWM mode (FPWM) or skip mode during the initial configuration. When the device is programmed to FPWM mode, light load switching behavior of each channel can be dynamically changed between FPWM and diode emulation(DE) individually. See *Section 8.3.4* for more detailed information.

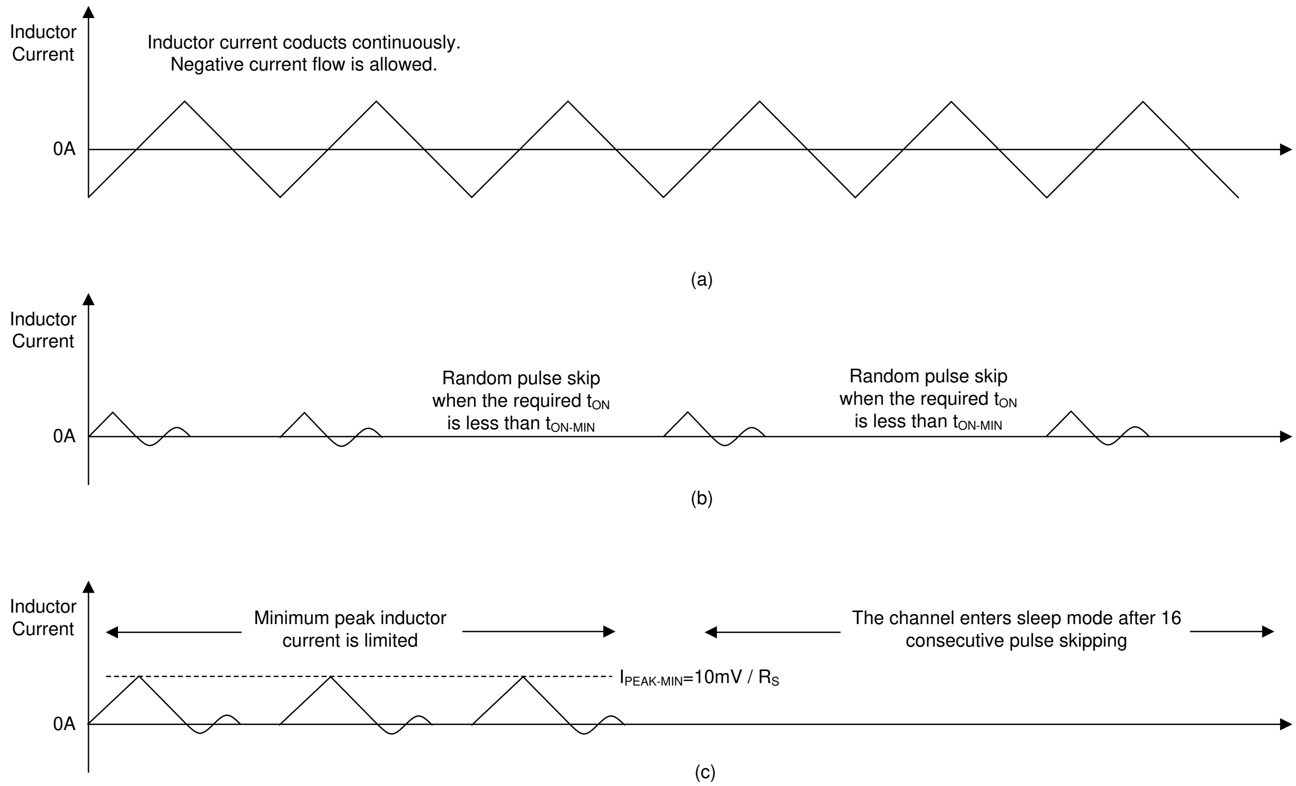


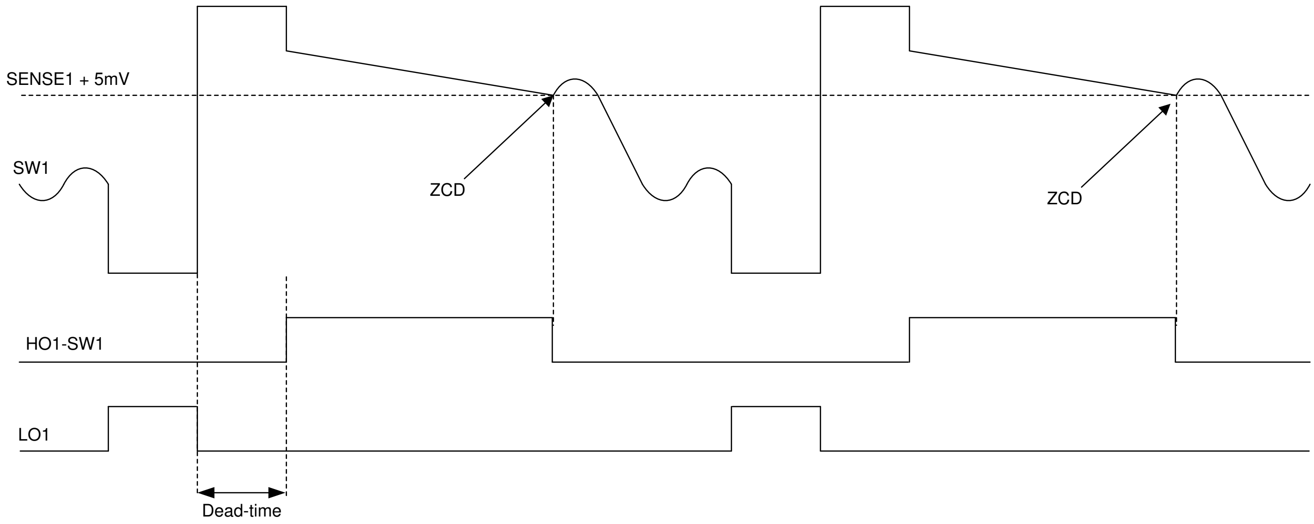
Figure 8-29. Inductor Current Waveform At Light Load (a) FPWM (b) Diode Emulation (DE) (c) Skip Mode

8.4.2.1 Forced PWM (FPWM) Operation

In FPWM, the inductor current conducts continuously at light or no load conditions, allowing a continuous conduction mode (CCM). The benefit of the forced PWM mode is the fast light load to heavy load transient response and constant frequency operation at light or no load conditions. The maximum reverse current is limited to 300 mV / $R_{DS(ON)}$ in the FPWM mode

8.4.2.2 Diode Emulation (DE) Operation (Connect R_{SS} at SS)

In the diode emulation operation, inductor current flow is allowed only in one direction; from the input source to the output load. Each channel can be dynamically and independently programmable between FPWM and DE by connecting 57.6 kΩ R_{SS} at the SS pin in parallel with C_{SS} in FPWM mode. In boost configuration, the device monitors the SENSE1-SW1 voltage during the high-side switch on-time and turns off the high-side switch when the SENSE1-SW1 voltage falls down below $V_{ZCD-BOOST}$. A reverse current flow through the high-side switch is prevented by latching off the high-side switch for the remainder of the PWM cycle. In buck configuration, the device monitors SW-PGND voltage during the low-side switch on-time and turns off the low-side switch when the SW-PGND voltage crosses over $V_{ZCD-BUCK}$. A reverse current flow through the low-side switch is prevented by latching off the low-side switch for the remainder of the PWM cycle. The main benefit of the diode emulation is to lower the power loss at light load conditions.



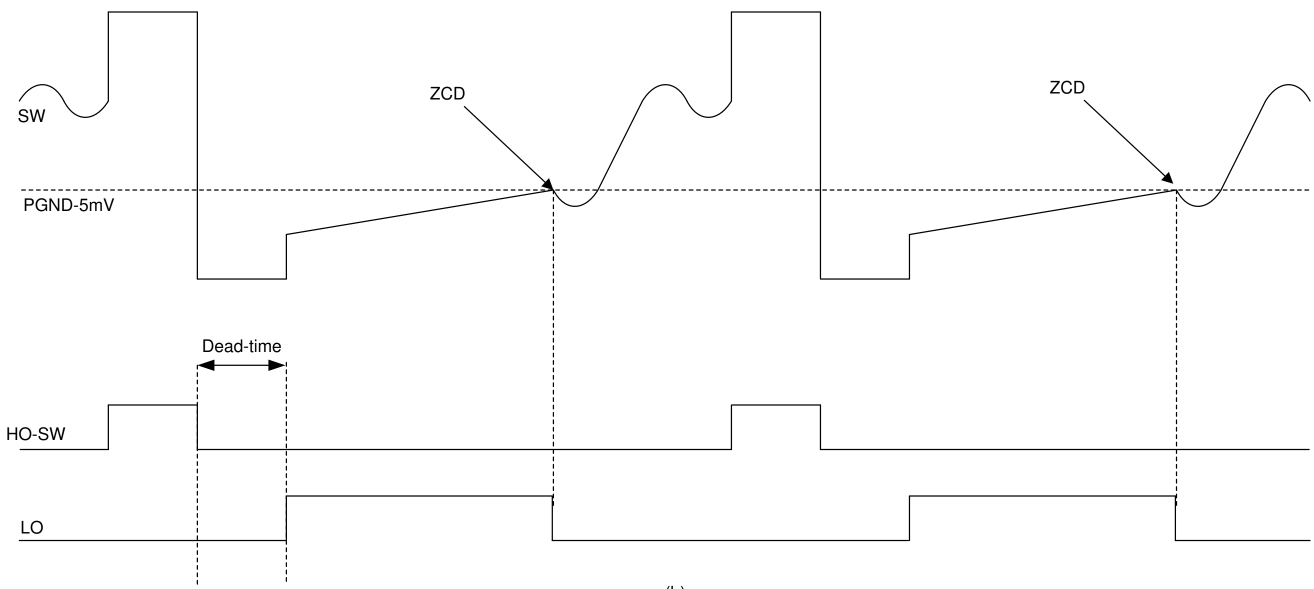


Figure 8-30. Zero Current Detection (a) Boost (b) Buck

8.4.2.3 Forced Diode Emulation Operation in FPWM Mode

During soft-start, the device forces diode emulation while the SS pin voltage is less than 1.5 V. When the SS pin is greater than 1.5 V, the device reduces the soft-start current to 2 µA and ramps the zero current detection (ZCD) threshold up/down to ±300 mV as shown in Figure 8-31, following the SS pin voltage in order to achieve a smooth transition from diode emulation to FPWM. It is important to keep the peak-to-peak inductor current x $R_{DS(ON)}$ / 2 less than 300 mV for a proper FPWM operation at no load.

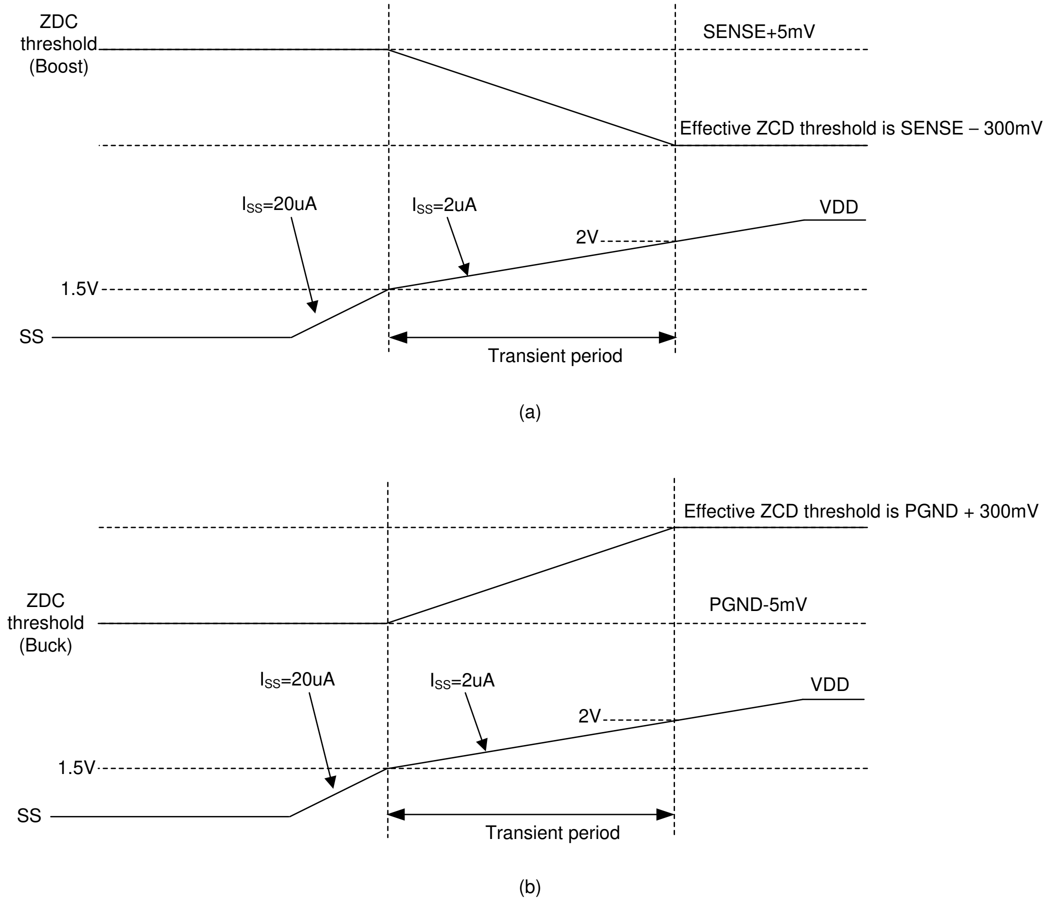


Figure 8-31. Dynamic Transition Between FPWM and Diode Emulation

8.4.2.4 Skip Mode Operation

The light load efficiency can be increased further by entering the sleep mode more frequently and staying in the sleep mode longer. In skip mode, the device works in diode emulation, but the minimum peak current is limited to 10 mV/R_S once the switch turns on. By limiting the minimum peak current, the converter supplies more current than the required, enters the sleep mode more frequently and stays longer in the sleep mode. In the skip mode configuration, the channel enters the sleep mode when the pulse skip counter detects 16 consecutive cycles of pulse skipping in active mode. Once the channel enters the sleep mode, the channel cannot re-enter the active mode during 4 µs + one cycle minimum sleep time. During the sleep mode, error amplifier is active and the FB monitor monitors the internal FB node. The channel enters active mode after a 5 µs delay if the COMP is greater than the COMP wake-up threshold ($V_{WAKE\text{-}COMP}$) or the internal FB is less than the FB wake-up threshold ($V_{WAKE\text{-}FB}$).

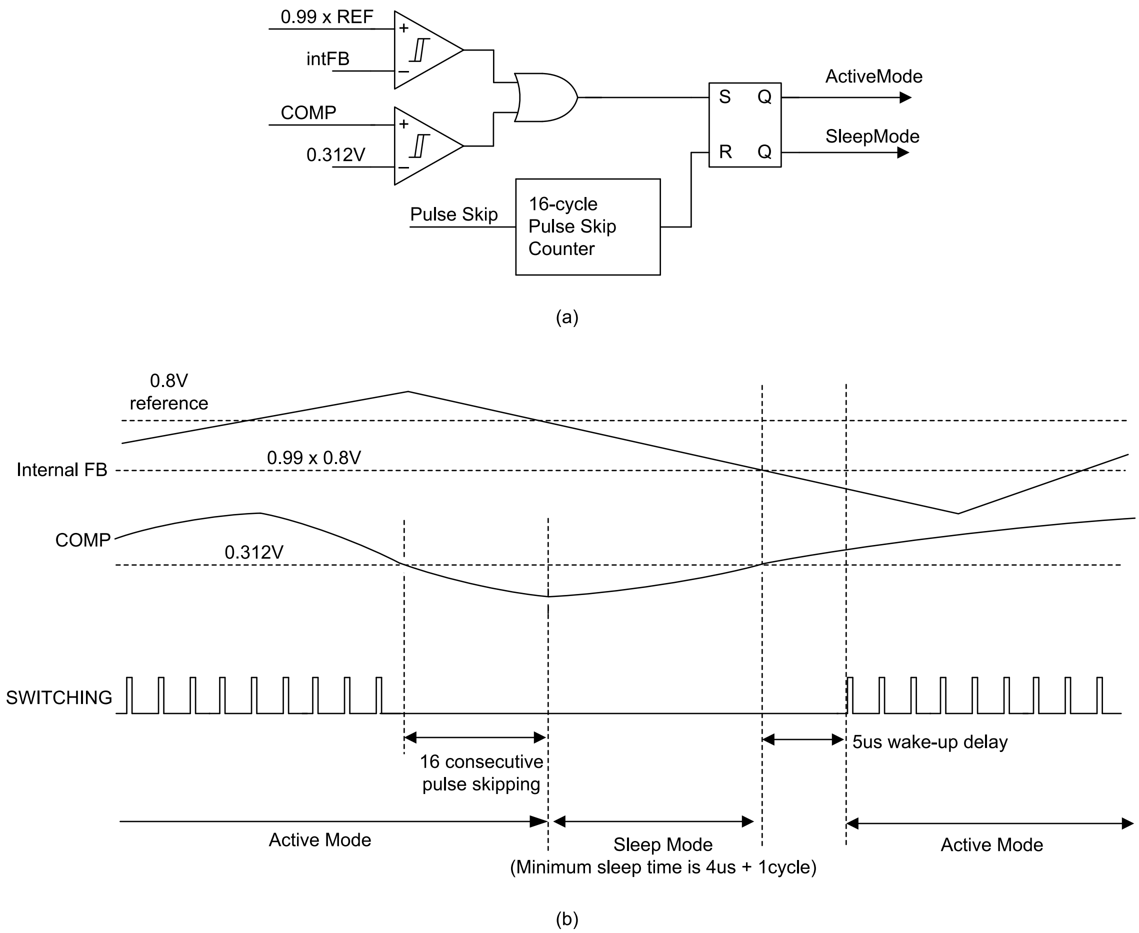


Figure 8-32. Skip Mode Operation (a) Sleep Mode Control (b) Waveforms

8.4.3 LM5127 Cheat Sheet

Table 8-11. LM5127 Cheat Sheet

DEVICE CONFIGURATON	NOTES
Boost/SEPIC + Buck + Buck	Configuration is latched during initial start-up.
Boost/SEPIC + 2PH Buck	Configuration is latched during initial start-up.
Buck + Buck + Buck	Configuration is latched during initial start-up.
Buck + 2PH Buck	Configuration is latched during initial start-up.
OUTPUT REGULATION SELECTION	**NOTES**
Fixed 3.3 V	Supported in buck. The regulation target is latched during initial start-up.
Fixed 5.0 V	Supported in buck. The regulation target is latched during initial start-up.
Adjustable from 0.8 to 42 V	Supported in boost and buck. Dynamically programmable during operation.
LIGHT LOAD SWITCHING MODE	**NOTES**
Skip mode	Apply to all channels. The mode is latched during initial start-up.
FPWM mode	Apply to all channels. The mode is latched during initial start-up.
DE operation in FPWM mode	Dynamically changeable between FPWM and DE during operation.
HICCUP MODE PROTECTION	**NOTES**
Hiccup mode protection	Apply to all channels. The mode is latched during initial start-up.
Latch-off mode protection	Apply to all channels. The mode is latched during initial start-up.
Cycle-by-cycle current limit	Apply to all channels. The mode is latched during initial start-up.
SWITCHING FREQUENCY	**NOTES**
RT programming	Apply to all channels. Dynamically programmable during operation.
SYNC	Apply to all channels. Dynamically programmable during operation. Dynamically changeable between SYNC and RT switching during operation.
DITHER	Apply to all channels. Dynamically programmable during operation. Dynamically changeable between DITHER and RT switching during operation.
FUNCTION	**NOTES**
Enable	Dedicated pin per channel
Soft-start	Dedicated pin per channel. SS3 is disabled in dual-phase buck.
PGOOD	Dedicated pin per channel. PGOOD3 is disabled in dual-phase buck.
DEVICE/CHANNEL STATUS	**NOTES**
Shutdown mode	Apply to all channels.
Configuration mode	Apply to all channels.
Active mode	Each channel works individually.
Sleep mode	Each channel works individually.
Deep sleep mode	Apply to all channels.
VCC HOLD mode	Apply to all channels.
PULSE WIDTH MODULATION TYPE	**NOTES**
Normal PWM operation	Available in both boost and buck.
Pulse skipping operation	Available in both boost and buck.
Bypass mode operation	Available in boost.
LDO mode operation	Available in buck.
SPECIAL DEVICE/CHANNEL STATUS	**NOTES**
Hiccup mode off	Each channel enters hiccup mode off individually. CH2 and CH3 enter hiccup mode off together in dual-phase buck. Automatic restart if hiccup mode is selected.
OVP protection	Each channel stops switching individually. Disabled in boost. Restarts naturally
Thermal Shutdown	All channels shutdown. Restarts naturally.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

TI provides application note which explaining how to design single boost, single buck and dual phase buck using the device. This comprehensive application note includes component selections and loop response optimization

See *How to Design Single Boost, Single Buck and Dual Phase Buck Using the LM5127* for more information.

9.2 Typical Application

Figure 9-1 shows typical application of the device. See *Section 9.3* for more system examples.

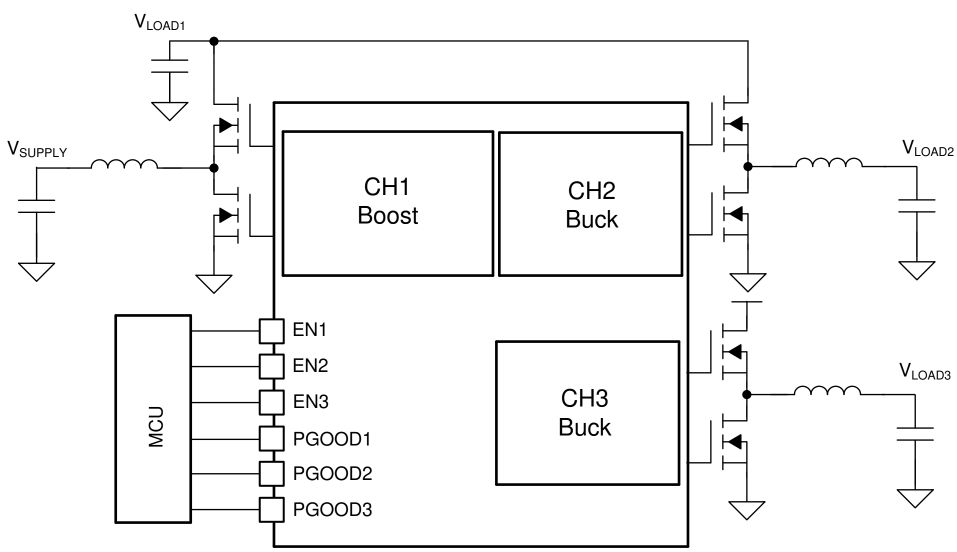


Figure 9-1. Pre-Boost + Two Single-phase Bucks

9.2.1 Design Requirements

Table 9-1 shows the intended input, output, and performance parameters for this application example.

Table 9-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Boost input voltage range (V_{SUPPLY})	3 V to 42 V (5 V required for start-up)
CH1 boost output voltage (V_{LOAD1})	6.8 V
CH2 buck output voltage (V_{LOAD2})	5.0 V
CH3 buck output voltage (V_{LOAD3})	3.3 V
CH1 maximum load current (I_{LOAD1})	10 A
CH2 maximum load current (I_{LOAD2})	5 A
CH3 maximum load current (I_{LOAD3})	7 A
Typical switching frequency (f_{SW})	440 kHz

9.2.2 Detailed Design Procedure

Use the Quick Start Calculator to expedite the process of designing of a regulator for a given application based on the LM5127-Q1 device. Download the LM5127 Quick Start Calculator for detailed design procedure.

See the LM5127EVM-FLEX Evaluation Module EVM user's guide for recommended components and typical application curves.

9.2.2.1 Recommended Power Tree Architecture

- It is strongly recommended to have at least one fixed 5-V rail and connect the 5 V output to the VCCX pin.
- If battery monitor is required, configure CH1 buck.
- If 3.3-V rail is required, program the VOUT3 to the fixed 3.3 V and utilize the VDDX function.
- SEPIC configuration is good when the load current is less than about 3 - 4 A. In the SEPIC configuration, the maximum input voltage has to be limited below 42 V - V_{VOUT1} since the SW node voltage is V_{SUPPLY} plus V_{LOAD} in the SEPIC configuration and switching noise should be considered.
- The maximum load current of the single buck channel can be up to about 20 A with proper thermal management.
- The maximum load current of the dual-phase buck can be up to about 40 A with proper thermal management.
- Cascaded configuration is allowed.
- The BIAS pin should be connected to the highest voltage rail in the system because the internal charge pump creates BIAS + 5 V rail for HB1. Especially, the BIAS pin should be connected to the output of the boost converter in boost configuration.
- Populate 100 pF C_{SS} if CH1 is used as a pre-boost.
- The CH2 buck input voltage can be higher or lower than the CH3 buck input voltage, but the BIAS pin should be always connected to the highest potential input voltage.

9.2.2.2 Application Ideas

For applications requiring the lowest cost with minimum conduction loss, inductor DC resistance (DCR) can be used to sense the inductor current rather than using a sense resistor. R_{DCRC} and C_{DCRC} must meet Equation 23 to match the time constant.

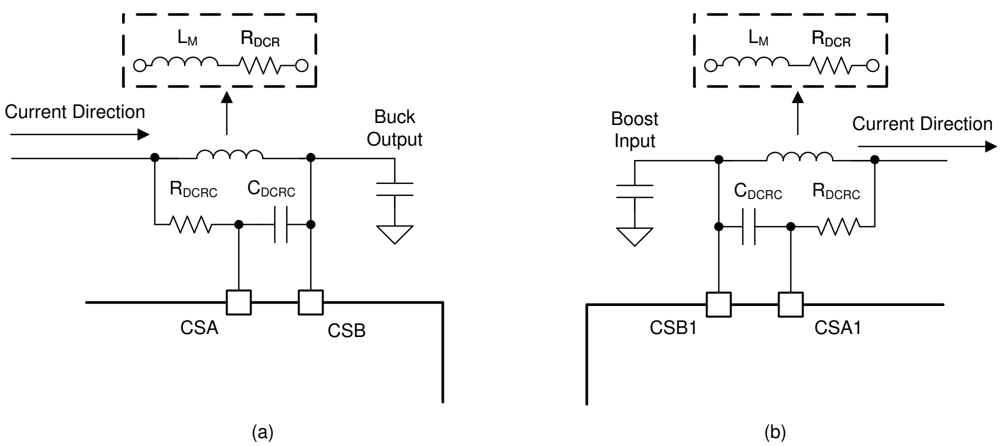


Figure 9-2. DCR Current Sensing (a) Buck, (b) Boost

$$\frac{L_M}{R_{DCR}} = R_{DCRC} \times C_{DCRC} \tag{23}$$

When CH1 is used as a pre-boost, the output undershoot during a cold-cranking event can be minimized by adding an R-C in parallel with the low-side feedback resistor. A lower value of R_{OS} will result in a lower output undershoot (see Figure 9-3). The C_{OS} value should be large enough not to affect loop response in normal operation. Use 20-kΩ and 4.7-nF combination as a starting point and then adjust the values if required.

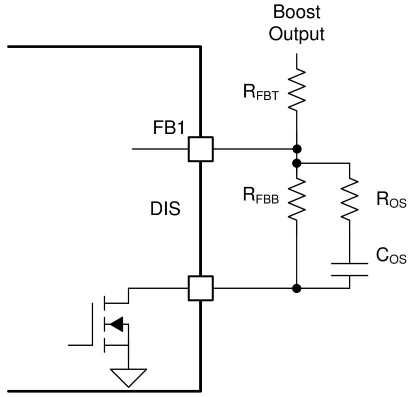


Figure 9-3. VOUT Boost Circuit

The light load switching mode can be dynamically programmed during operation between FPWM and DE mode.

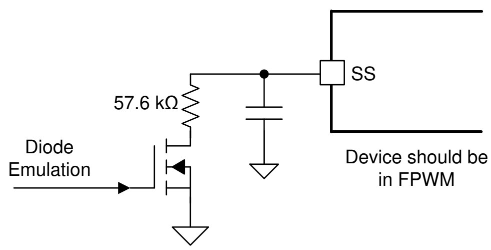


Figure 9-4. Dynamic Transition Between FPWM and DE

If required, an additional PGOOD or BMOUT delay can be programmed using an external circuit.

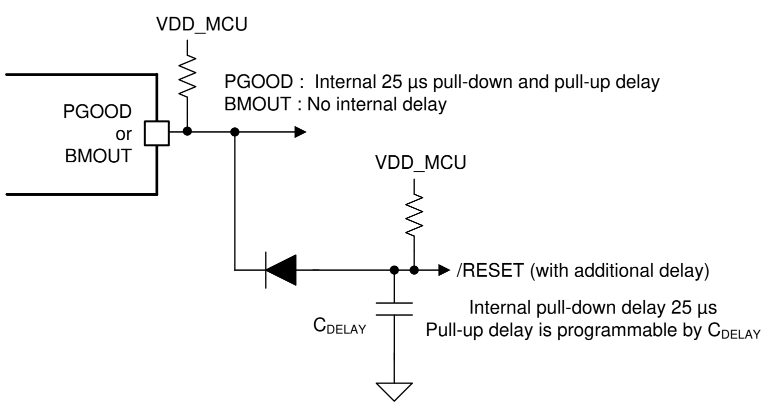


Figure 9-5. Additional PGOOD / BMOUT Delay

Sequential start-up can be realized by using the PGOOD pins.

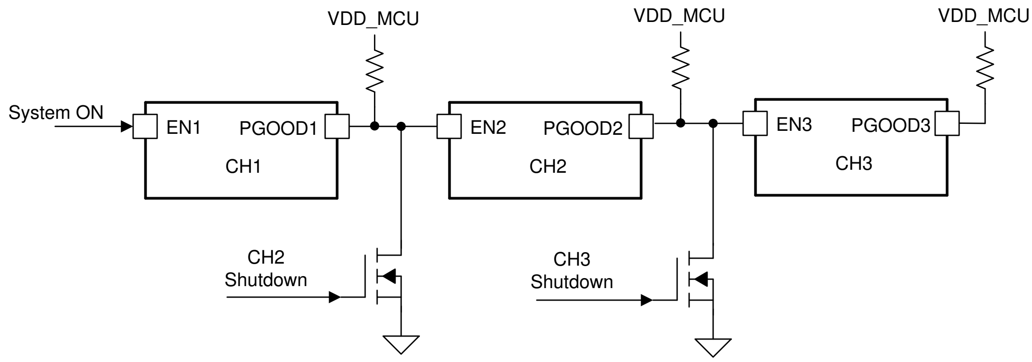


Figure 9-6. Sequential Start-up

Switching can be stopped individually by pulling down the SS pins.

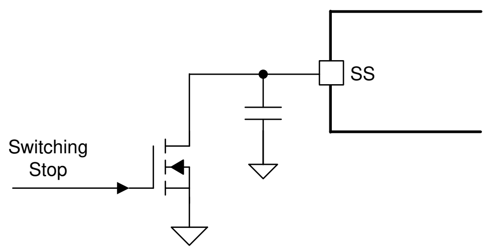


Figure 9-7. Stop Switching using SS Pin

9.2.3 Application Curves

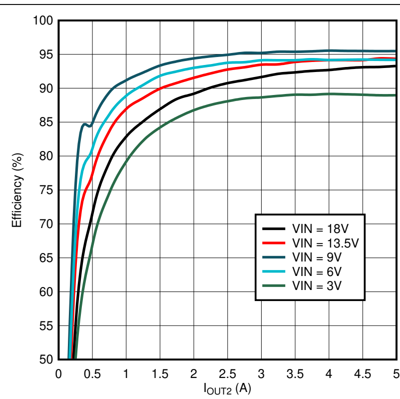


Figure 9-8. Efficiency vs. I_{OUT2} (FPWM)

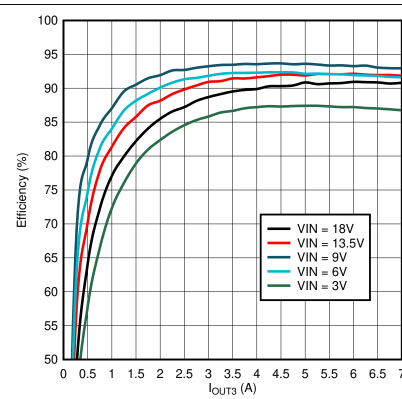


Figure 9-9. Efficiency vs. I_{OUT3} (FPWM)

9.3 System Examples

The BIAS and the SENSE1 pins should be connected to the output of the boost converter in this pre-boost + two single buck configuration.

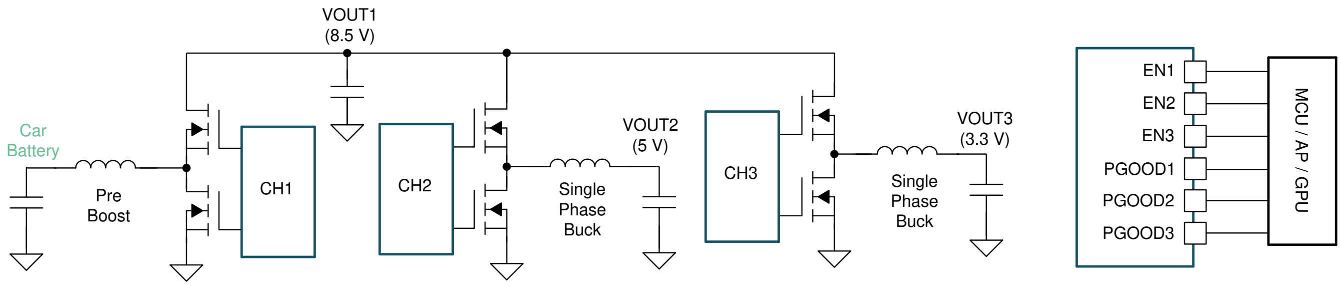


Figure 9-10. Pre-Boost + Two Single-phase Bucks Configuration

The BIAS and the SENSE1 pins should be connected to the output of the boost converter in this pre-boost + dual-phase buck configuration.

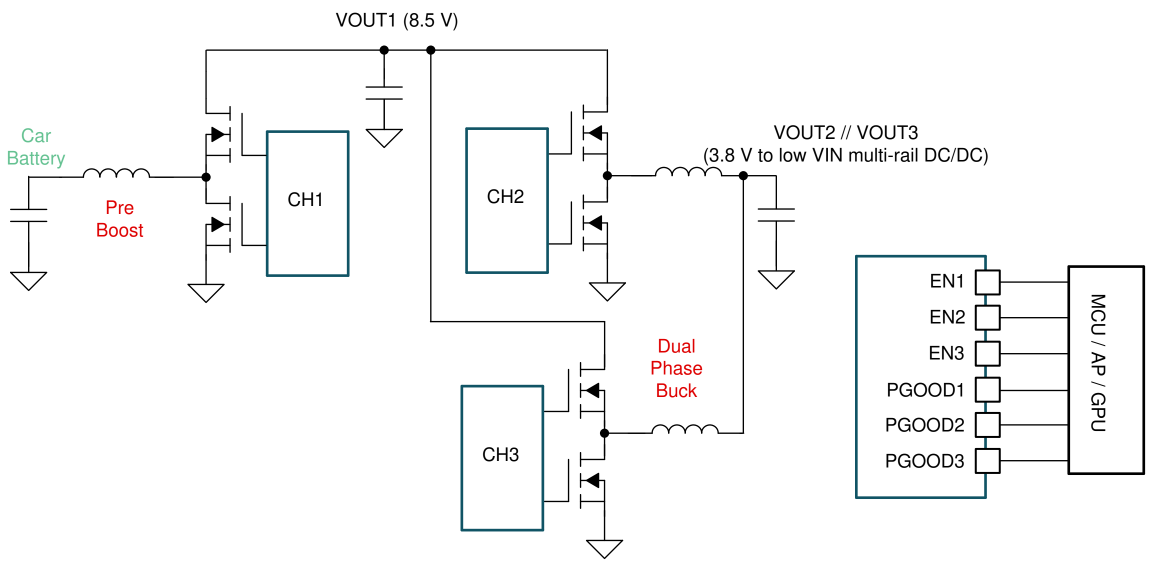


Figure 9-11. Pre-Boost + Dual-phase Buck Configuration

The BIAS pin should be connected to the input of the buck converter in this three single buck configuration.

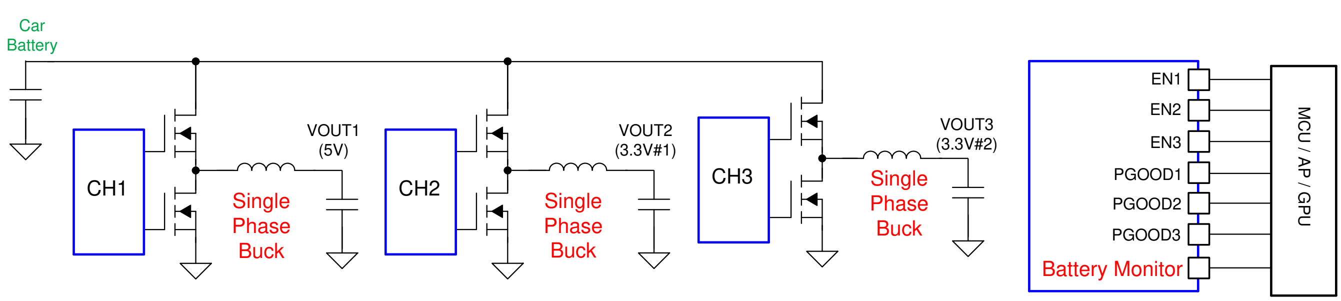


Figure 9-12. Three Single-phase Bucks + Battery Monitor Configuration

The BIAS pin should be connected to the input of the buck converter in this dual-phase buck + single buck configuration.

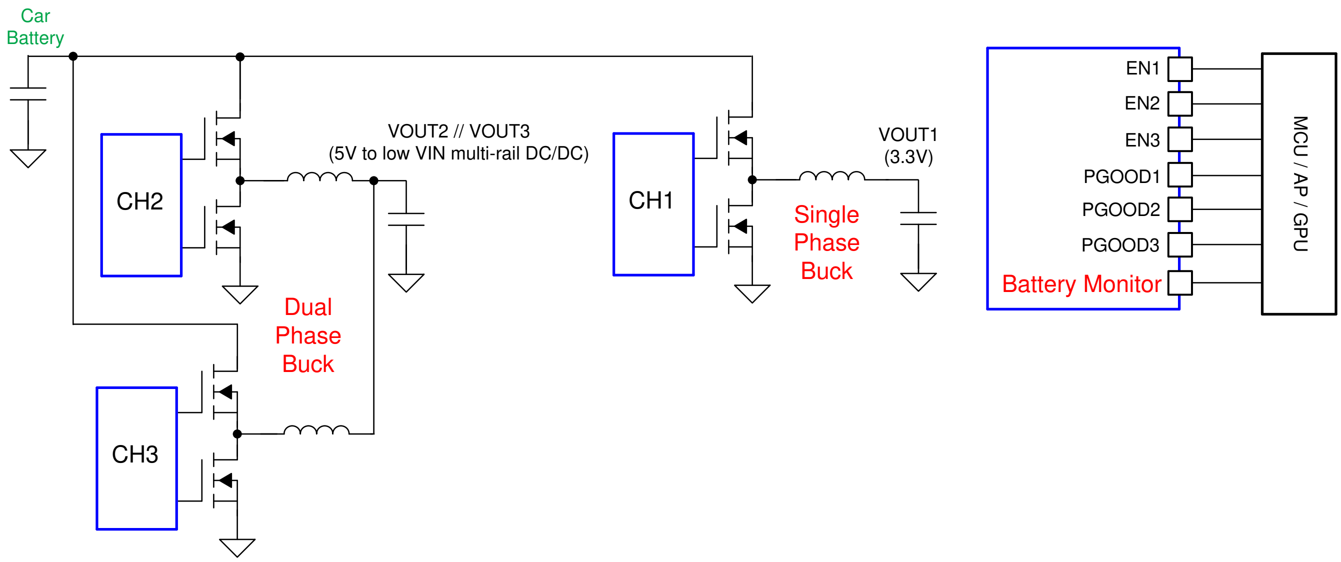


Figure 9-13. Dual-phase Buck + Single-phase Buck + Battery Monitor Configuration

The BIAS and the SENSE1 pins should be connected to the output of the boost converter in this configuration.

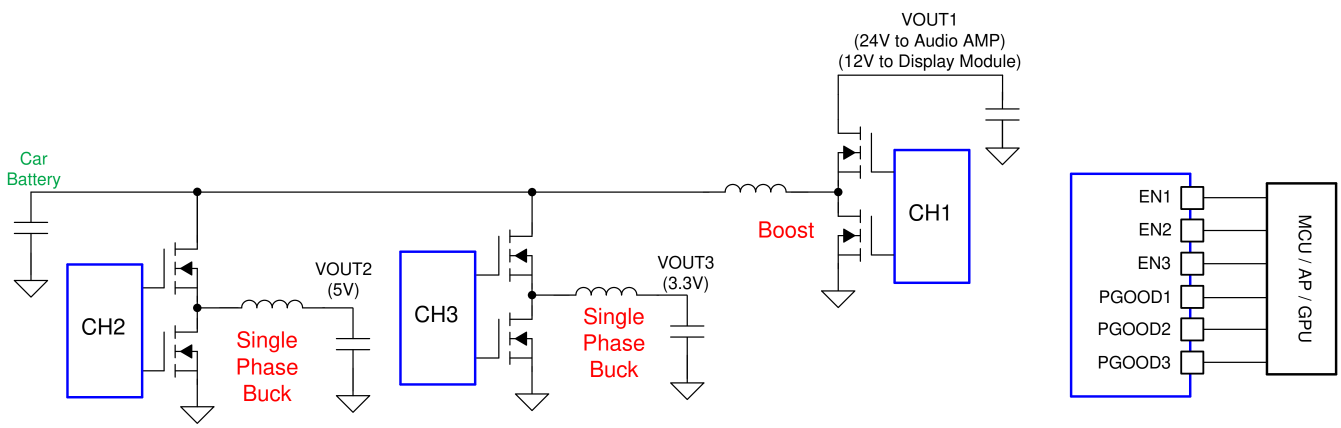


Figure 9-14. Two Single-phase Bucks in Parallel with Boost Configuration

The BIAS and the SENSE1 pins should be connected to the buck converter input. The SW1 pins should be connected to the PGND1 pin. HO1 pin can be left floating. The HB1 pin should be connected to the VCC pin in non-synchronous boost configuration.

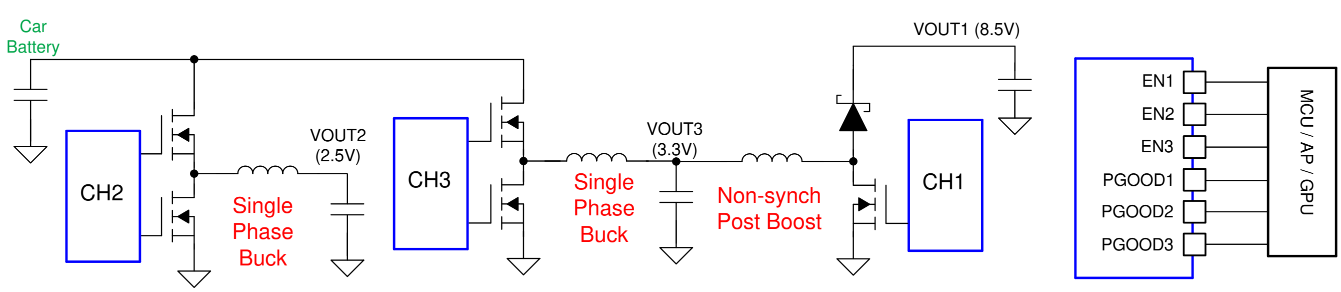


Figure 9-15. Two Single-phase Bucks + Non-Synchronous Post-Boost Configuration

The BIAS pin should be connected to the buck converter input. The SENSE1 and SW1 pins should be connected to the PGND1 pin. HO1 should be connected to the high-side MOSFET through an AC coupling capacitor. HB1 should be connected to VCC in this synchronous SEPIC configuration.

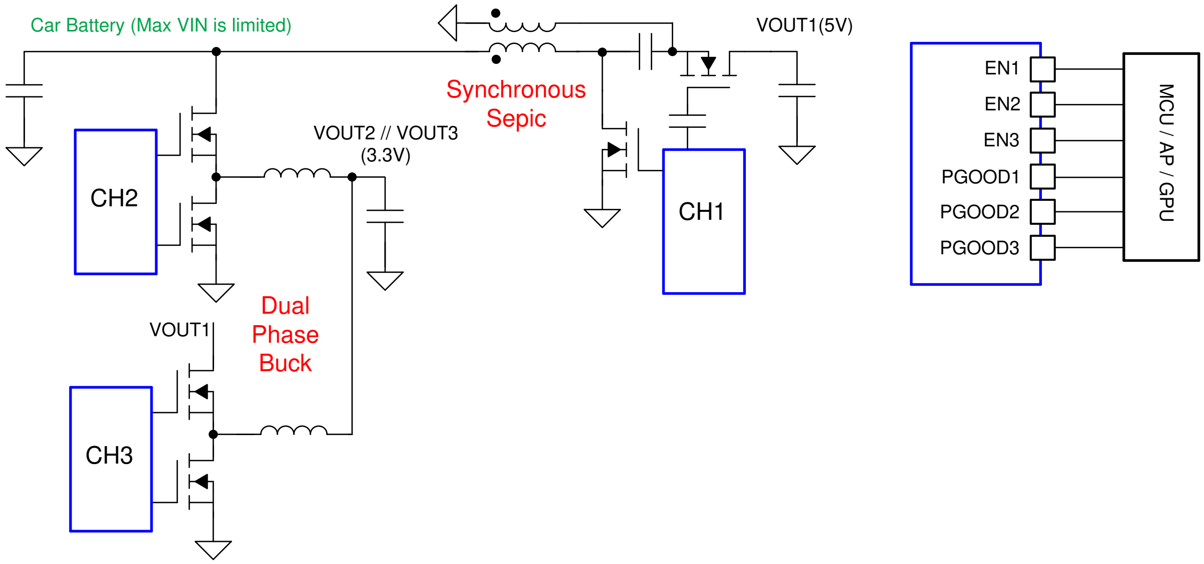


Figure 9-16. Dual-phase Buck in Parallel with Synchronous SEPIC Configuration

10 Power Supply Recommendations

The device is designed to operate from a power supply or a battery whose voltage range is from 0.8 V to 42 V. The input power supply must be able to supply the maximum boost supply voltage and handle the maximum input current at 0.8 V. The impedance of the power supply and battery including cables must be low enough that an input current transient does not cause an excessive voltage drop. Additional input ceramic capacitors may be required at the supply input of the converter.

11 Layout

11.1 Layout Guidelines

These items must be applied to every channel.

- Populate the device on the top layer.
- Connect the PGND1, PGND2, and PGND3 pins to the DAP directly on the top layer.
- Populate a common 10-µF VCC capacitor between VCC and DAP on the bottom layer.
- Use a differential mode filters (100 Ω and 220 pF) at CSA-CSB. Connect the 100 Ω to CSA.
- Route CSA and CSB traces in parallel.
- Populate 0.1-µF HB capacitors between HB and SW on the top layer.
- Connect the SENSE1 pin to the drain connection of the high-side MOSFET in boost.
- Connect the SENSE1 pin to the output in SEPIC topology.
- Connect a 1-µF BIAS capacitor between BIAS and ground.
- Connect a 0.1-µF VDD capacitor between VDD and AGND.
- Connect the loop compensation components between COMP to AGND.

These items must be applied to every buck channel.

- Populate 0.1-µF local VCC capacitors between VCC and PGND on the top layer.
- Populate local boot diodes (Schottky diode) from the positive connection of the local VCC capacitors to the positive connection of the HB capacitors on the top layer.
- Populate minimum 1.5-Ω gate resistors from HO to the gate of high-side MOSFET and populate pull-down PNP transistors in parallel.
- Populate minimum 1.5-Ω gate resistors from LO to the gate of low-side MOSFET and populate pull-down PNP transistors in parallel.
- Use the low-side MOSFET whose $r_{DS(on)}$ is greater than 8 mΩ at the room temperature.
- Connect the source connection of the low-side MOSFET to PGND directly with minimum 2.5-mm width trace (length < 0.8 inch).
- Connect the drain connection of the low-side MOSFET to SW directly with minimum 2.5-mm width trace (length < 0.8 inch).
- Route SW and PGND in parallel.

These items must be applied when CH2 and CH3 are configured as a dual-phase interleaved buck.

- Place two R_S resistors as close as possible.
- Place a ceramic output capacitor from the midpoint between two resistors and output ground.

11.2 Layout Example

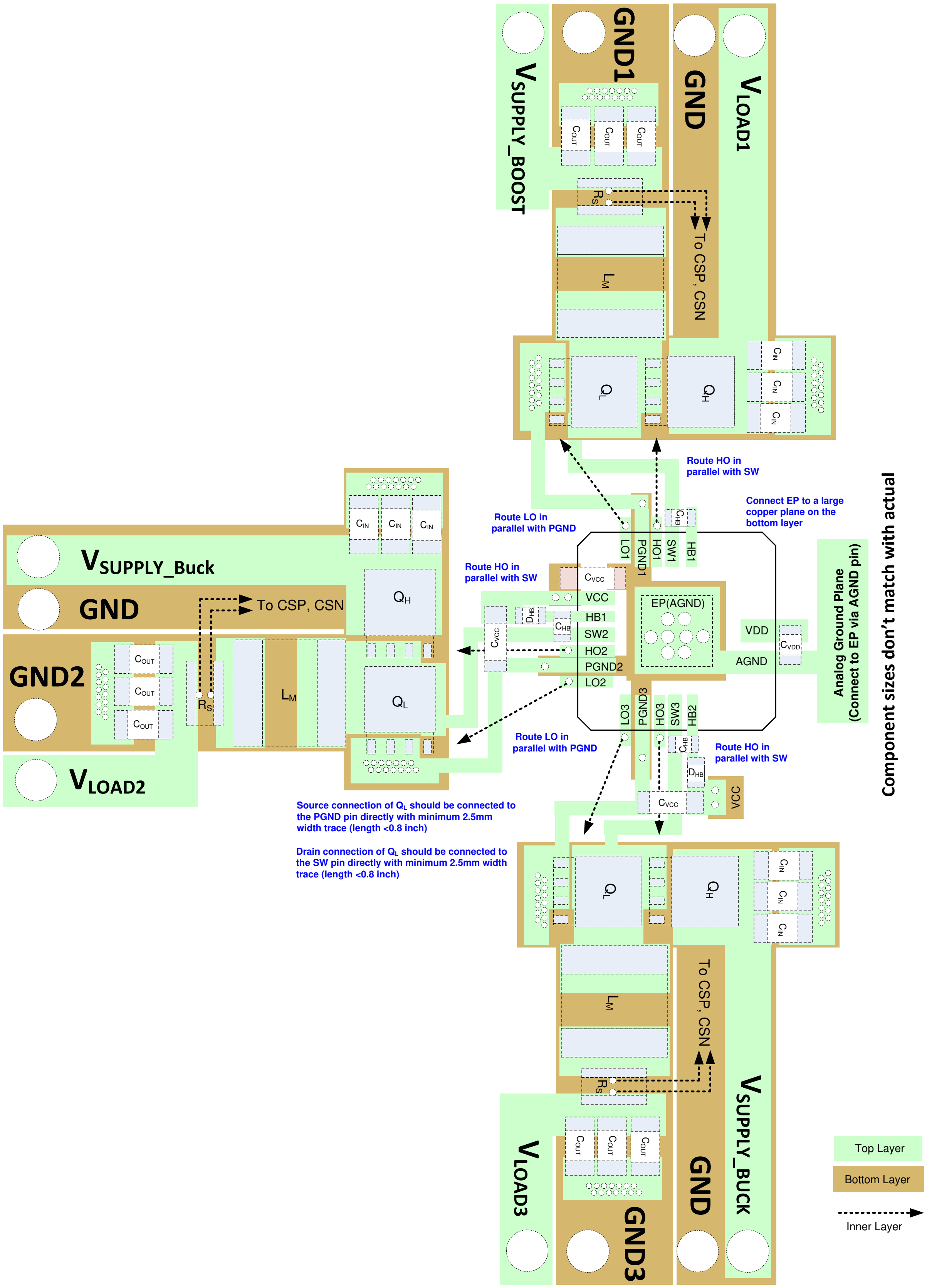


Figure 11-1. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

For development support see the following:

- *LM5127-Q1 Quick Start Calculator*
- *How to Design Single Boost, Single Buck and Dual Phase Buck Using the LM5127*

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, *LM5127EVM-FLEX Evaluation Module*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5127QRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 150	LM5127Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

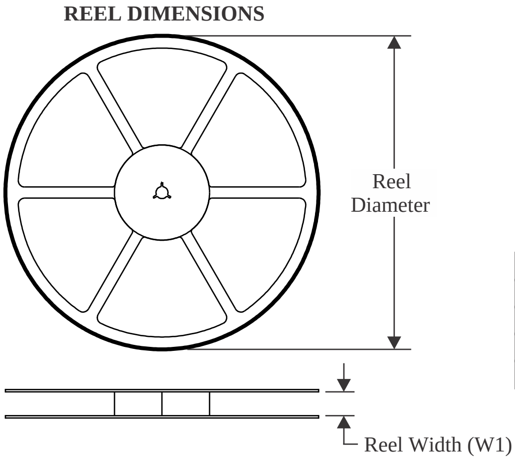
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

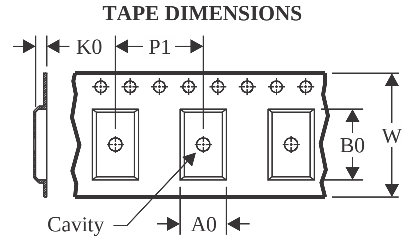
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

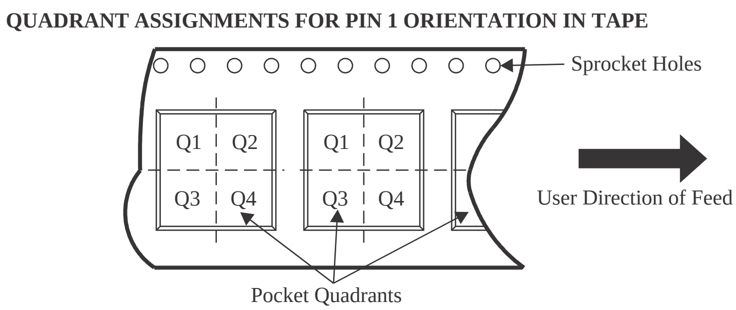
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





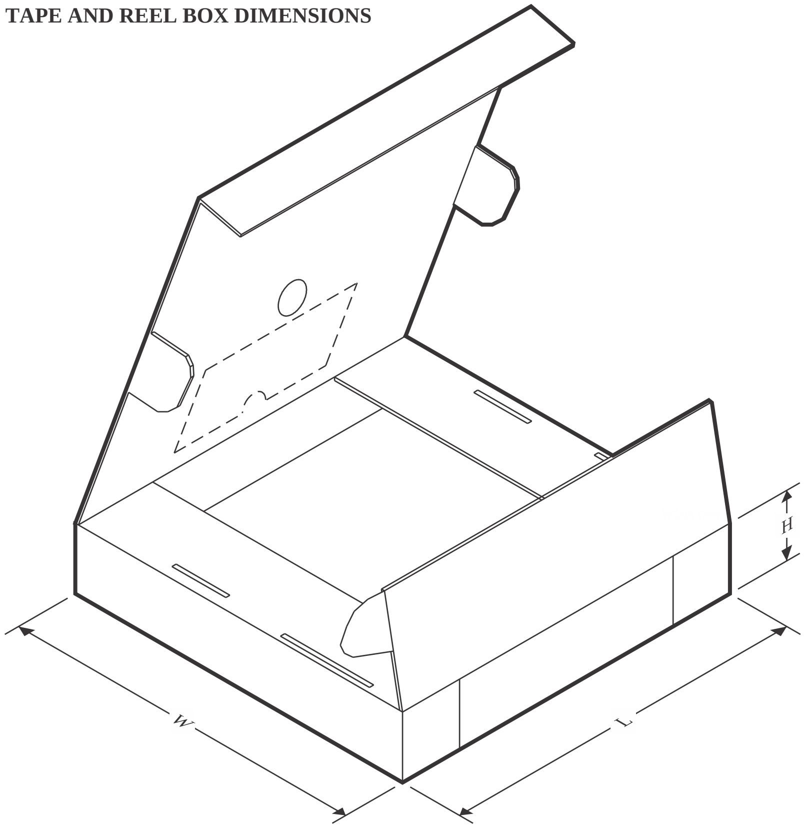
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5127QRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

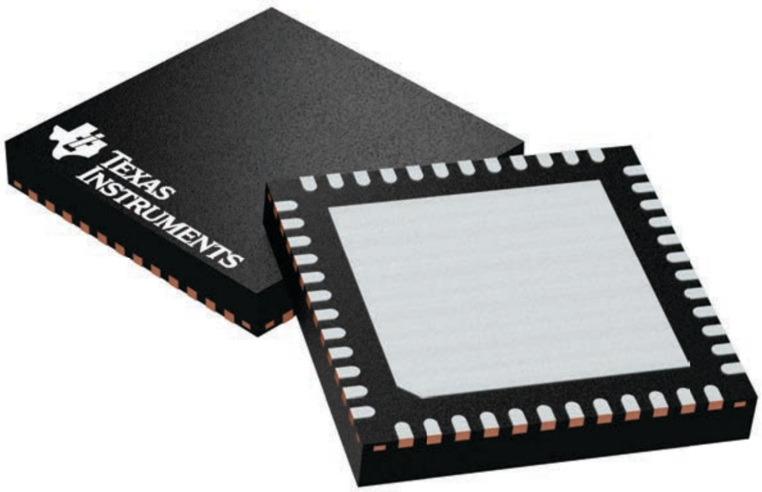
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5127QRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	35.0

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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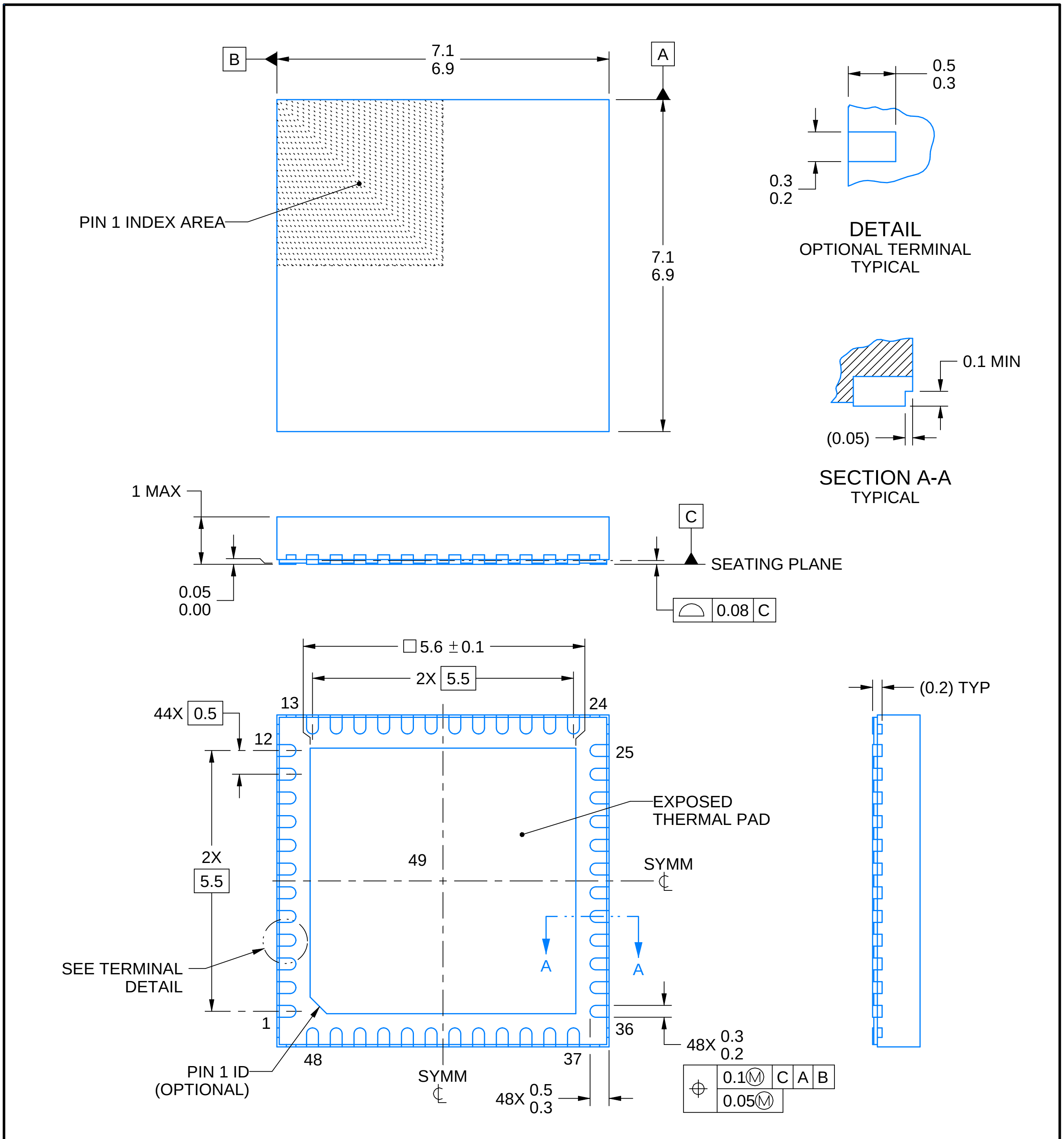

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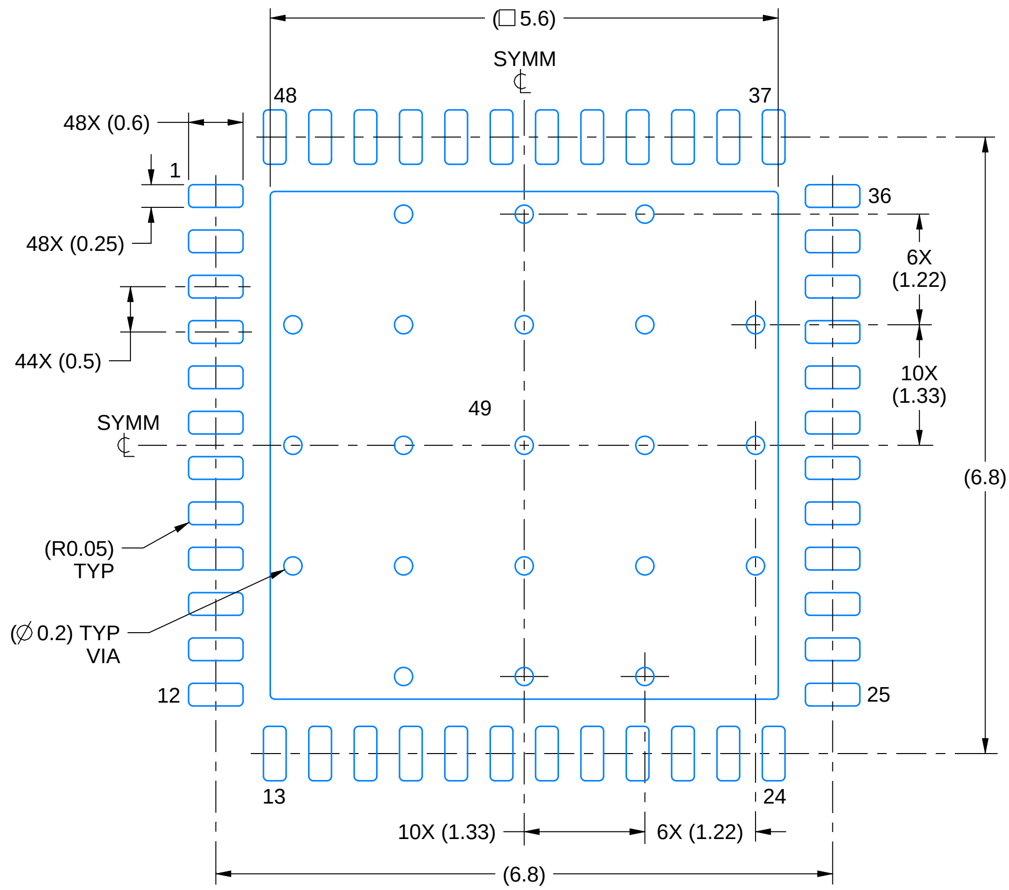
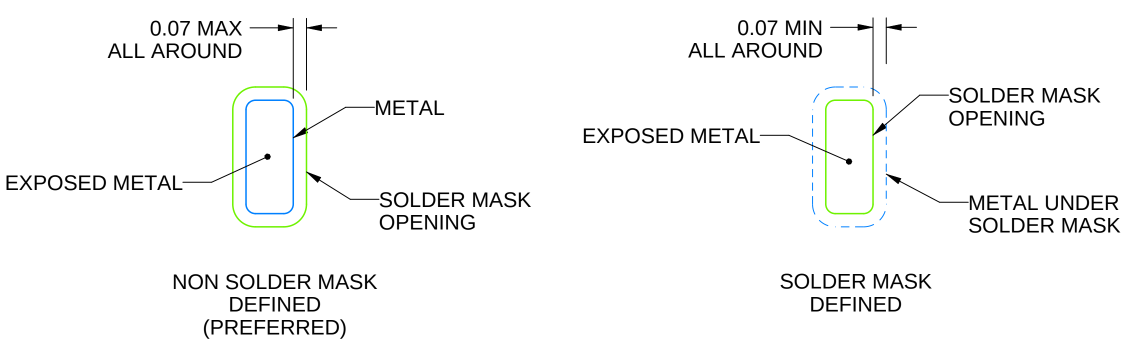
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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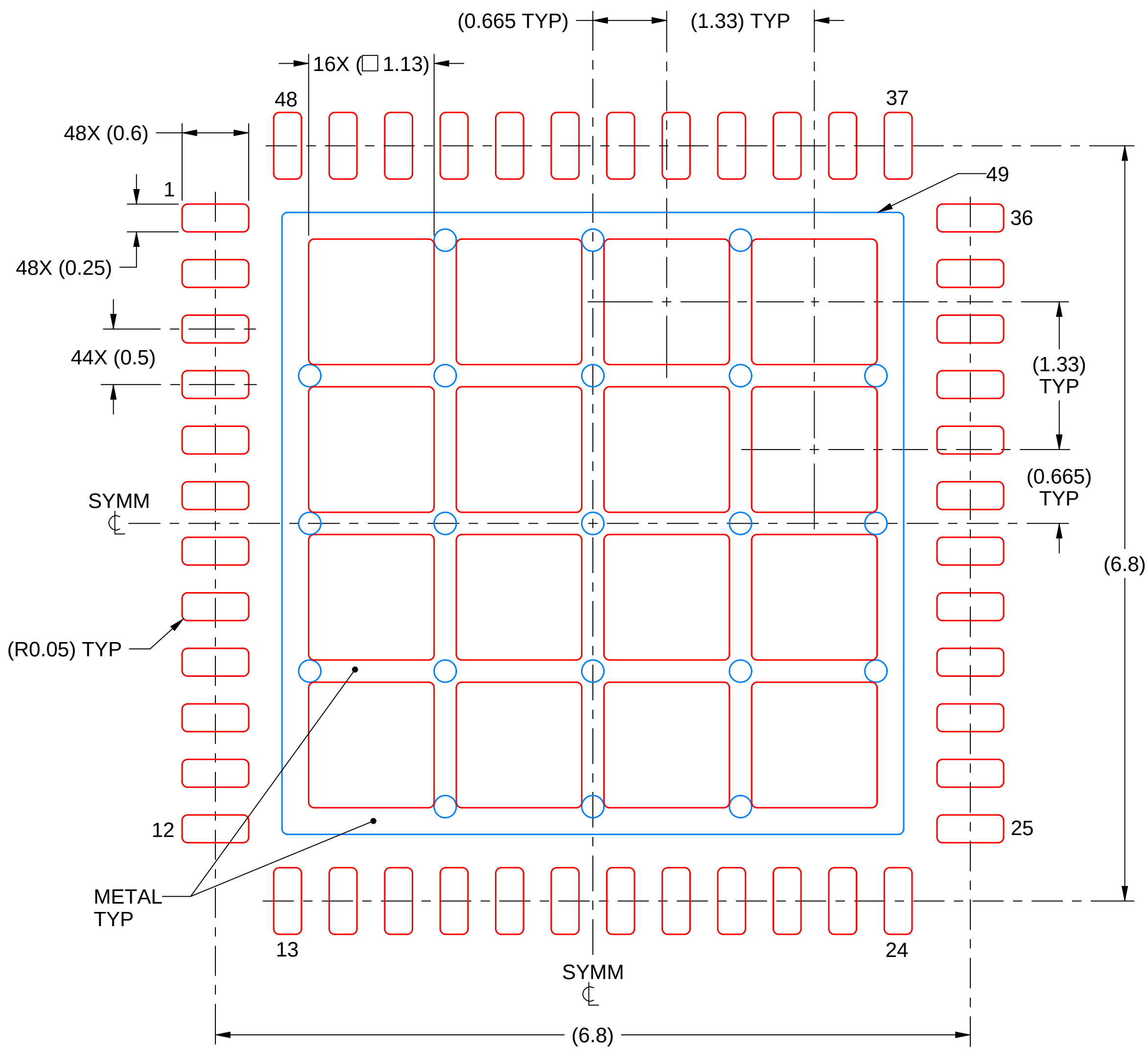
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.