

# Pulsed-Load Synchronous Regulator with Bypass Mode for GSM PA Supply, TINYBOOST<sup>®</sup>, 2.5 MHz, 2.0 A

## FAN48632

### Description

The FAN48632 allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The FAN48632 is a boost regulator designed to provide a minimum output voltage ( $V_{OUT(MIN)}$ ) from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 1.5 A continuous and 2.0 A pulsed. Quiescent current in Shutdown Mode is less than 3  $\mu$ A, which maximizes battery life. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current.

The FAN48632 is available in a 16-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

### Features

- Few External Components: 0.47  $\mu$ H Inductor and 0603 Case Size Input and Output Capacitors
- Input Voltage Range: 2.35 V to 5.5 V
- Fixed Output Voltage: 3.3 V to 3.5 V
- Maximum Continuous Load Current of: 1.5 A at  $V_{IN}$  of 2.6 V
- Maximum Pulsed Load Current of: 2.0 A for GSM 217 Hz Repetition Rate, boosting  $V_{OUT}$  to 3.3 V or 3.5 V
- Up to 96% Efficient
- True Bypass Operation when  $V_{IN} >$  Target  $V_{OUT}$
- Internal Synchronous Rectifier
- Soft-Start with True Load Disconnect
- Forced Bypass Mode
- $V_{SEL}$  Control to Optimize Target  $V_{OUT}$
- Short-Circuit Protection
- Low Operating Quiescent Current
- 16-Bump, 0.4 mm Pitch WLCSP
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Boost for Low-Voltage Li-ion Batteries, Brownout Prevention, Supply GSM RF PA
- Cell Phones, Smart Phones, Tablets



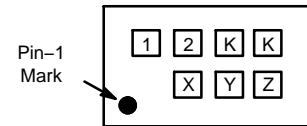
ON Semiconductor<sup>®</sup>

[www.onsemi.com](http://www.onsemi.com)



WLCSP16 1.78x1.78x0.586  
CASE 567SY

### MARKING DIAGRAM



- 12 = Alphanumeric Device Marking
- KK = Lot Run Code
- X = Alphabetical Year Code
- Y = 2-weeks Date Code
- Z = Assembly Plant Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

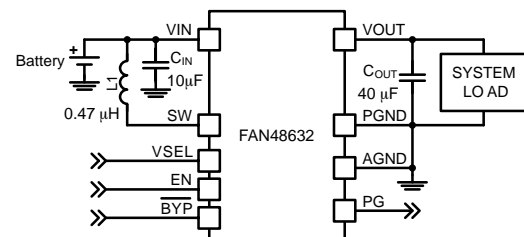


Figure 1. Typical Application

# FAN48632

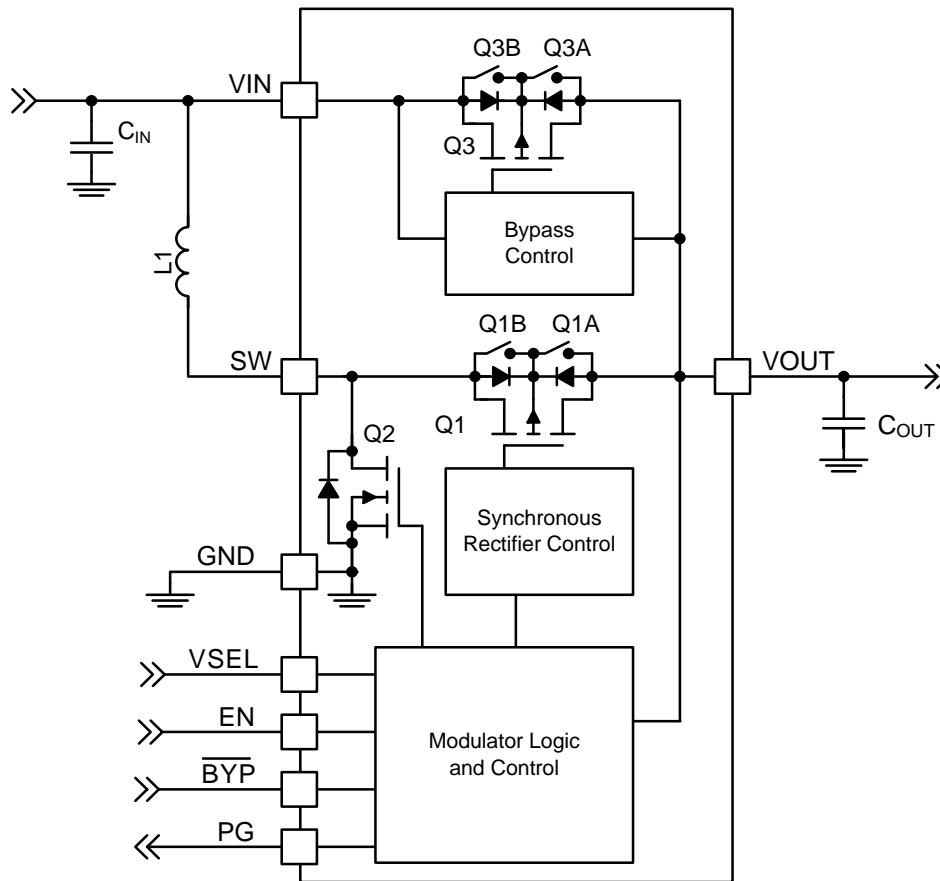
**Table 1. ORDERING INFORMATION**

Part Number	Output Voltage $V_{SELO}/V_{SEL1}$	Soft – Start	Forced Bypass	Operating Temperature	Package	Shipping†
FAN48632UC33X	3.30 / 3.49	FAST	Low $I_Q$	–40 to 85°C	16-Ball, 4x4 Array, 0.4 mm Pitch, 250 $\mu$ m Ball, Wafer-Level Chip-Scale Package (WLCSP)	3000 / Tape & Reel
FAN48632BUC33X (Note 1)	3.30 / 3.49	FAST	Low $I_Q$			
FAN48632UC35X	3.50 / 3.70	FAST	Low $I_Q$			

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. The FAN48632BUC33X includes backside lamination.

## TYPICAL APPLICATION



**Figure 2. Block Diagram**

**Table 2. RECOMMENDED COMPONENTS**

Component	Description	Vendor	Parameter	Typ.	Unit
$L_1$	0.47 $\mu$ H, 30%	Toko: DFE201612C DFR201612C Cynotec: PIFE20161B	L	0.47	$\mu$ H
			DCR (Series R)	40	m $\Omega$
$C_{IN}$	10 $\mu$ F, 10%, 10 V, X5R, 0603	TDK: C1608X5R1A106K	C	10	$\mu$ F
$C_{OUT}$	2 x 22 $\mu$ F, 20%, 6.3 V, X5R, 0603	TDK: C1608X5R0J226M	C	44	$\mu$ F

PIN CONFIGURATION

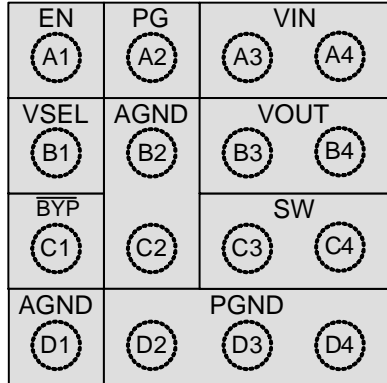


Figure 3. Top Through View (Bumps Down)

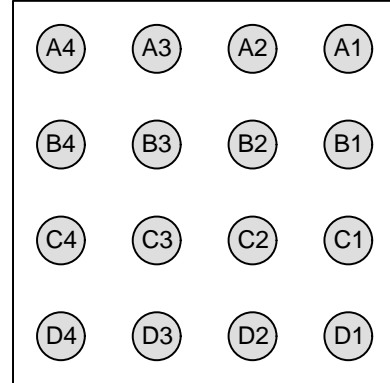


Figure 4. Bottom View (Bumps Up)

Table 3. PIN DEFINITIONS

Pin #	Name	Description
A1	EN	<b>Enable.</b> When this pin is HIGH, the circuit is enabled (Note 2).
A2	PG	<b>Power Good.</b> This is an open-drain output. PG is actively pulled LOW if output falls out of regulation due to overload or if thermal protection threshold is exceeded.
A3–A4	VIN	<b>Input Voltage.</b> Connect to Li-Ion battery input power source (Note 2).
B1	VSEL	<b>Output Voltage Select.</b> When boost is running, this pin can be used to select output voltage.
B2, C2, D1	AGND	<b>Analog Ground.</b> This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
B3–B4	VOUT	<b>Output Voltage.</b> Place C <sub>OUT</sub> as close as possible to the device.
C1	BYP	<b>Bypass.</b> This pin can be used to activate Forced Bypass Mode. When this pin is LOW, the bypass switches (Q3 and Q1) are turned on and the IC is otherwise inactive.
C3–C4	SW	<b>Switching Node.</b> Connect to inductor.
D2–D4	PGND	<b>Power Ground.</b> This is the power return for the IC. The C <sub>OUT</sub> bypass capacitor should be returned with the shortest path possible to these pins.

2. The EN pin can be tied to VIN, but it is recommended to tie EN to the 1.8 V logic voltage.

**Table 4. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Min.	Max.	Unit	
V <sub>IN</sub>	V <sub>IN</sub> Input Voltage	-0.3	6.5	V	
V <sub>OUT</sub>	V <sub>OUT</sub> Output Voltage		6.0	V	
	SW Node				
	DC	-0.3	8.0	V	
	Transient: 10 ns, 3 MHz	-1.0	8.0	V	
	Other Pins	-0.3	6.5 (Note 3)	V	
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114		3.0	kV
		Charged Device Model per JESD22-C101		1.5	kV
T <sub>J</sub>	Junction Temperature	-40	+150	°C	
T <sub>STG</sub>	Storage Temperature	-65	+150	°C	
T <sub>L</sub>	Lead Soldering Temperature, 10 Seconds		+260	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Lesser of 6.5 V or V<sub>IN</sub> + 0.3 V.

**Table 5. RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IN</sub>	Supply Voltage	2.35	5.5	V
I <sub>OUT</sub>	Output Current	0	1500	mA
T <sub>A</sub>	Ambient Temperature	-40	+85	°C
T <sub>J</sub>	Junction Temperature	-40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 6. THERMAL CHARACTERISTICS**

Symbol	Parameter	Typ.	Unit
θ <sub>JA</sub>	Junction-to-Ambient Thermal Resistance	80	°C/W
θ <sub>JB</sub>	Junction-to-Board Thermal Resistance	42	

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer ON Semiconductor evaluation boards (1 oz copper on all layers). Special attention must be paid not to exceed junction temperature T<sub>J(max)</sub> at a given ambient temperature T<sub>A</sub>.

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**Table 7. ELECTRICAL CHARACTERISTICS**

Recommended operating conditions, unless otherwise noted, circuit per Figure 1,  $V_{IN} = 2.35\text{ V}$  to  $V_{OUT}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ . Typical values are given  $V_{IN} = 3.0\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_Q$	$V_{IN}$ Quiescent Current	Bypass Mode $V_{OUT} = 3.5\text{ V}$ , $V_{IN} = 4.2\text{ V}$		140	190	$\mu\text{A}$
		Boost Mode $V_{OUT} = 3.5\text{ V}$ , $V_{IN} = 2.5\text{ V}$		150	250	$\mu\text{A}$
		Shutdown: $EN = 0$ , $V_{IN} = 3.0\text{ V}$		1.5	5.0	$\mu\text{A}$
		Forced Bypass Mode $V_{IN} = 3.5\text{ V}$	Low $I_Q$		4	10
$I_{LK}$	$V_{OUT}$ to $V_{IN}$ Reverse Leakage	$V_{OUT} = 5\text{ V}$ , $EN = 0$		0.2	1.0	$\mu\text{A}$
$I_{LK\_OUT}$	$V_{OUT}$ Leakage Current	$V_{OUT} = 0$ , $EN = 0$ , $V_{IN} = 4.2\text{ V}$		0.1	1.0	$\mu\text{A}$
$V_{UVLO}$	Under-Voltage Lockout	$V_{IN}$ Rising		2.20	2.35	V
$V_{UVLO\_HYS}$	Under-Voltage Lockout Hysteresis			200		mV
$V_{PG(OL)}$	PG Low	$I_{PG} = 5\text{ mA}$			0.4	V
$I_{PG\_LK}$	PG Leakage Current	$V_{PG} = 5\text{ V}$			1	$\mu\text{A}$
$V_{IH}$	Logic Level High $EN$ , $VSEL$ , $\overline{BYP}$		1.2			V
$V_{IL}$	Logic Level Low $EN$ , $VSEL$ , $\overline{BYP}$				0.4	V
$R_{LOW}$	Logic Control Pin Pull Downs (LOW Active)	$\overline{BYP}$ , $VSEL$ , $EN$		300		$\text{k}\Omega$
$I_{PD}$	Weak Current Source Pull-Down	$\overline{BYP}$ , $VSEL$ , $EN$		100		nA
$V_{REG}$	Output Voltage Accuracy	Target $V_{OUT}$ relative to GND, DC, $V_{OUT} - V_{IN} > 100\text{ mV}$	-2		4	%
$V_{TRSP}$	Load Transient Response	500–1250 mA, $V_{IN} = 3.0\text{ V}$		$\pm 4$		%
$t_{ON}$	On-Time	$V_{IN} = 3.0\text{ V}$ , $V_{OUT} = 3.5\text{ V}$ , Load $> 1\text{ A}$		80		ns
$f_{SW}$	Switching Frequency	$V_{IN} = 3.0\text{ V}$ , $V_{OUT} = 3.5\text{ V}$ , Load $= 1\text{ A}$	2.0	2.5	3.0	MHz
$I_{V\_LIM}$	Boost Valley Current Limit	$V_{IN} = 2.6\text{ V}$	3.3	3.7	4.1	A
$I_{V\_LIM\_SS}$	Boost Valley Current Limit During SS	$V_{IN} = 2.6\text{ V}$		1.8		A
$I_{SS\_PK}$	Soft-Start Input Peak Current Limit	LIN1	Fast	900		mA
		LIN2	Fast	1800		mA
$t_{SS}$	Soft-Start $EN$ HIGH to Regulation	Fast, $50\ \Omega$ Load		600		$\mu\text{s}$
$V_{OVP}$	Output Over-Voltage Protection Threshold			6.0	6.3	V
$V_{OVP\_HYS}$	Output Over-Voltage Protection Hysteresis			300		mV
$R_{DS(ON)N}$	N-Channel Boost Switch $R_{DS(ON)}$	$V_{IN} = 3.5\text{ V}$		85	120	$\text{m}\Omega$
$R_{DS(ON)P}$	P-Channel Sync Rectifier $R_{DS(ON)}$	$V_{IN} = 3.5\text{ V}$		65	85	$\text{m}\Omega$
$R_{DS(ON)P\_BYP}$	P-Channel Bypass Switch $R_{DS(ON)}$	$V_{IN} = 3.5\text{ V}$		65	85	$\text{m}\Omega$
$T_{120A}$	T120 Activation Threshold			120		$^\circ\text{C}$
$T_{120R}$	T120 Release Threshold			100		$^\circ\text{C}$
$T_{150T}$	T150 Threshold			150		$^\circ\text{C}$
$T_{150H}$	T150 Hysteresis			20		$^\circ\text{C}$
$t_{RST}$	FAULT Restart Timer			20		ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

Unless otherwise specified;  $V_{IN} = 3.0\text{ V}$ ,  $V_{OUT} = 3.5\text{ V}$ ,  $V_{SEL} = 0\text{ V}$ , and  $T_A = 25^\circ\text{C}$ ; circuit and components according to Figure 1.

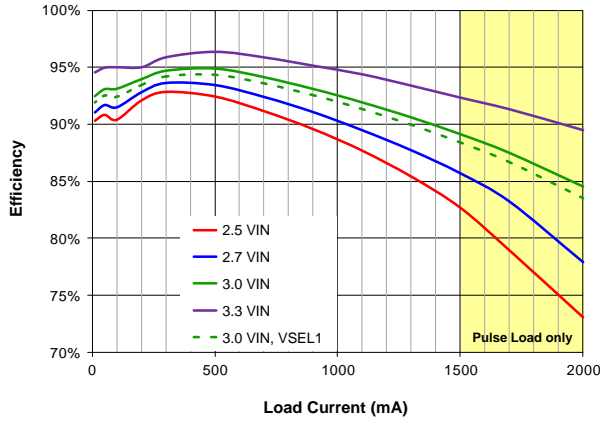


Figure 5. Efficiency vs. Load Current and Input Voltage

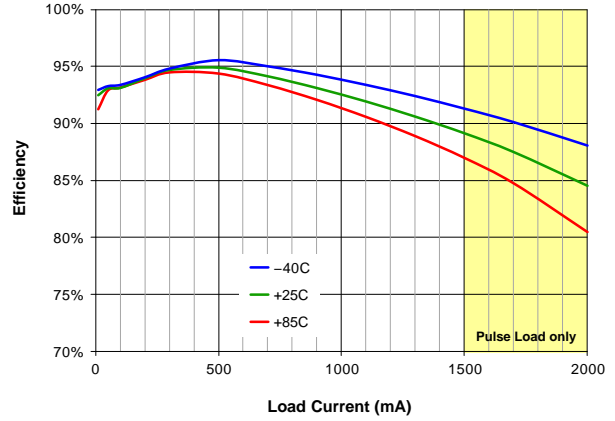


Figure 6. Efficiency vs. Load Current and Temperature

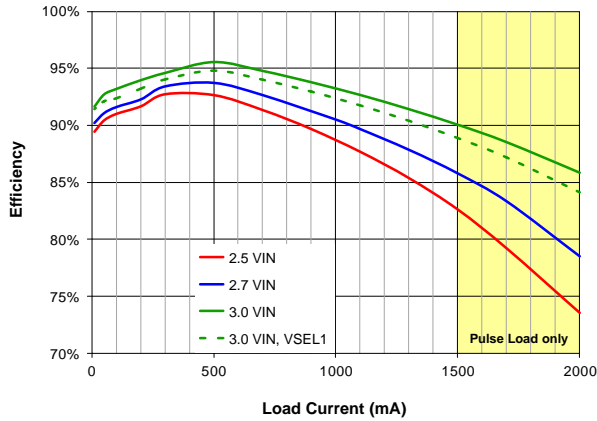


Figure 7. Efficiency vs. Load Current and Input Voltage,  $V_{OUT} = 3.3\text{ V}$

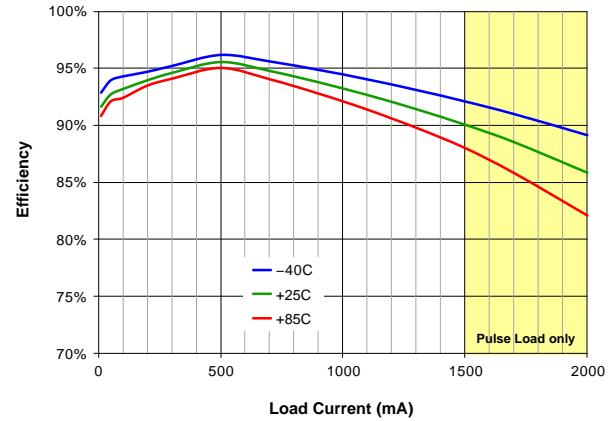


Figure 8. Efficiency vs. Load Current and Temperature,  $V_{OUT} = 3.3\text{ V}$

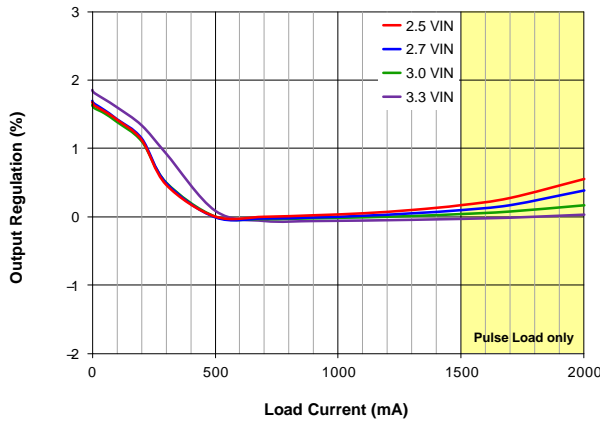


Figure 9. Output Regulation vs. Load Current and Input Voltage (Normalized to  $3.0\text{ V}_{IN}$ ,  $500\text{ mA}$  Load)

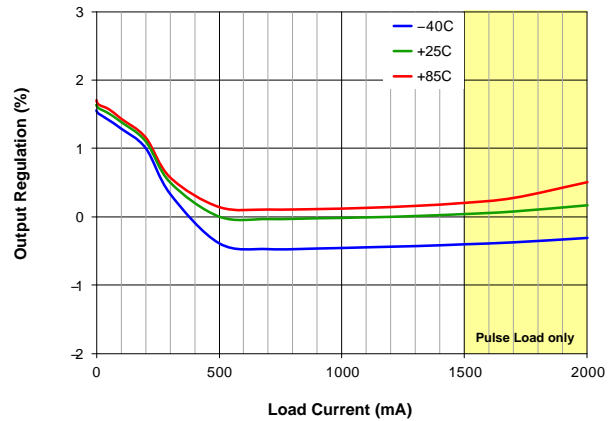


Figure 10. Output Regulation vs. Load Current and Temperature (Normalized to  $3.0\text{ V}_{IN}$ ,  $500\text{ mA}$  Load,  $T_A = 25^\circ\text{C}$ )

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified;  $V_{IN} = 3.0\text{ V}$ ,  $V_{OUT} = 3.5\text{ V}$ ,  $V_{SEL} = 0\text{ V}$ , and  $T_A = 25^\circ\text{C}$ ; circuit and components according to Figure 1.

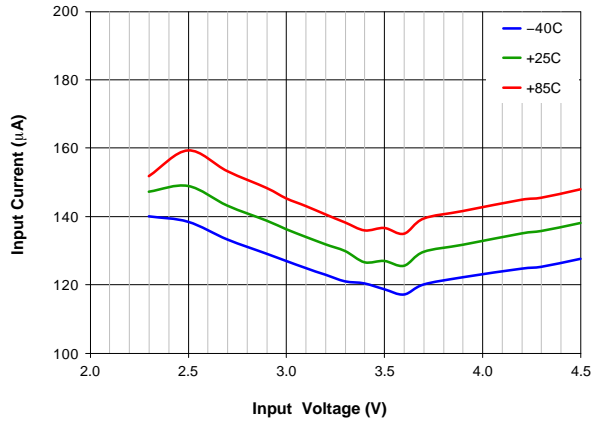


Figure 11. Quiescent Current vs. Input Voltage and Temperature, Auto Bypass

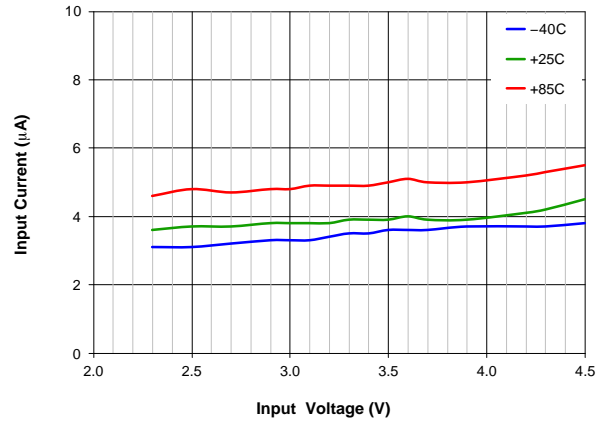


Figure 12. Quiescent Current vs. Input Voltage, Temperature, Forced Bypass (Low  $I_Q$ )

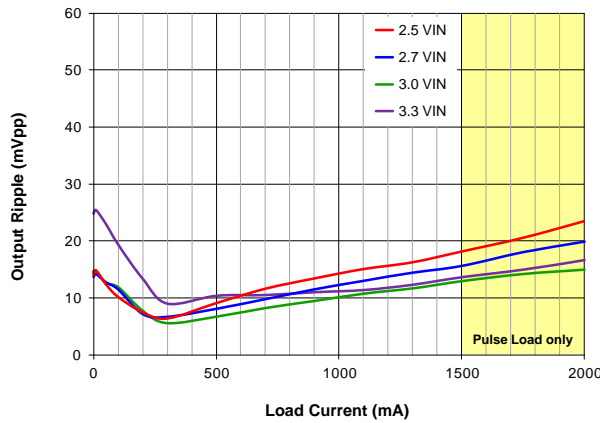


Figure 13. Output Ripple vs. Load Current and Input Voltage

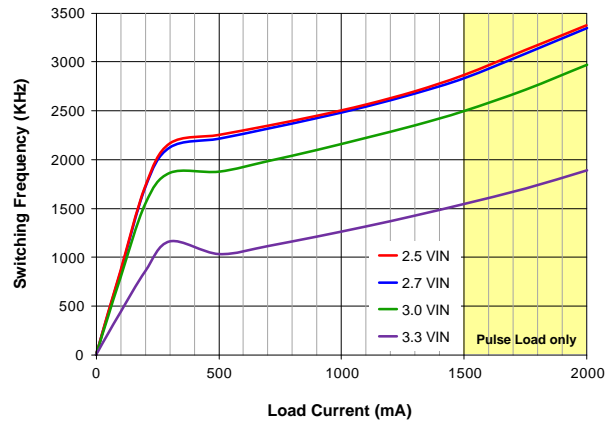


Figure 14. Switching Frequency vs. Load Current and Input Voltage

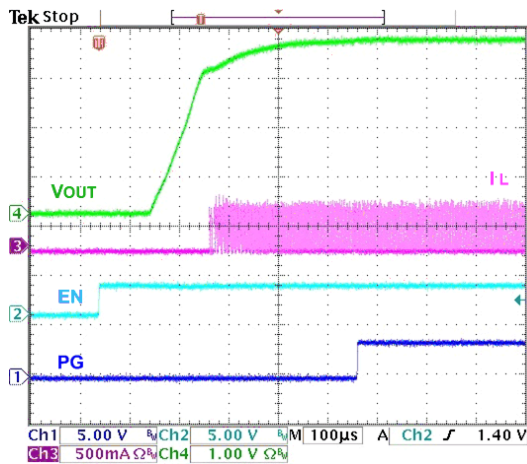


Figure 15. Startup, 50  $\Omega$  Load

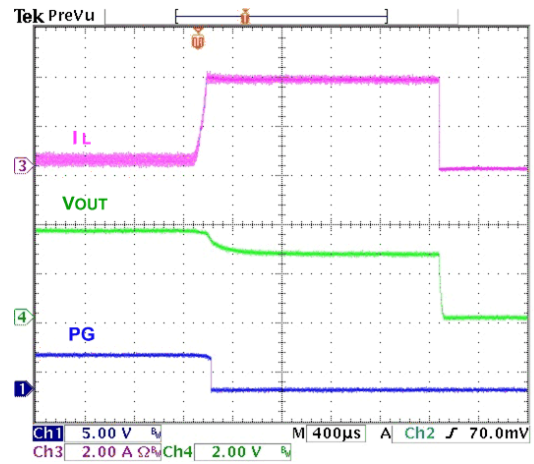


Figure 16. Overload Protection

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified;  $V_{IN} = 3.0\text{ V}$ ,  $V_{OUT} = 3.5\text{ V}$ ,  $V_{SEL} = 0\text{ V}$ , and  $T_A = 25^\circ\text{C}$ ; circuit and components according to Figure 1.

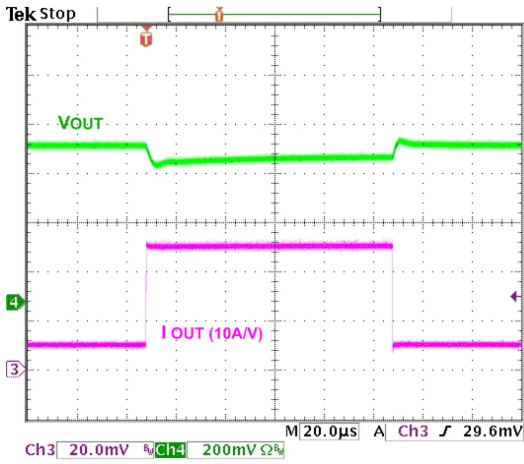


Figure 17. Load Transient, 100–500 mA, 100 ns Edge

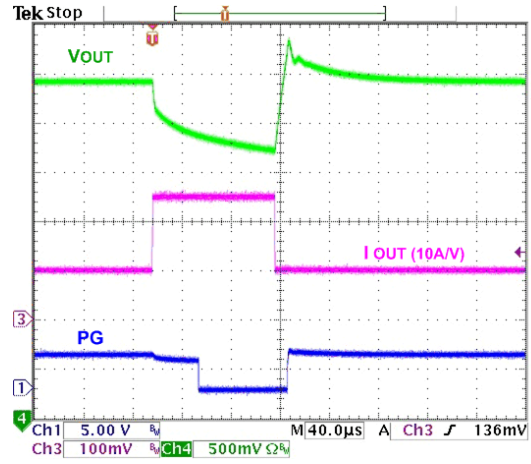


Figure 18. Transient Overload, 1.0–2.5 A, 100 ns Edge

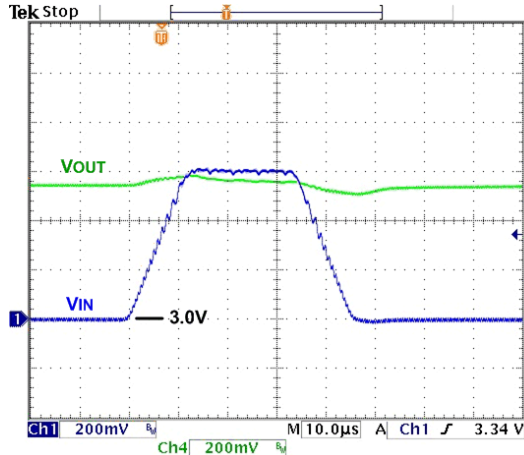


Figure 19. Line Transient, 3.0–3.6  $V_{IN}$ , 10  $\mu\text{s}$  Edge, 1.0 A Load

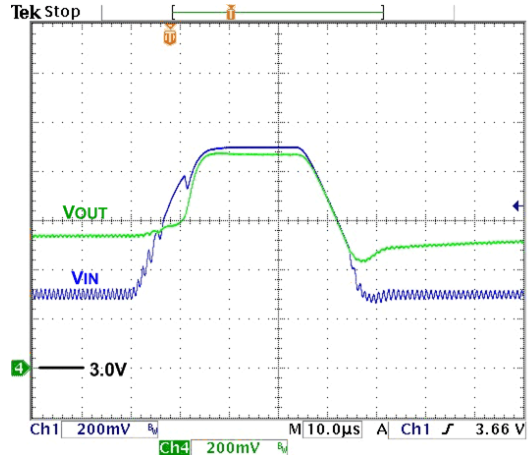


Figure 20. Line Transient, 3.3–3.9  $V_{IN}$ , 10  $\mu\text{s}$  Edge, 1.0 A Load

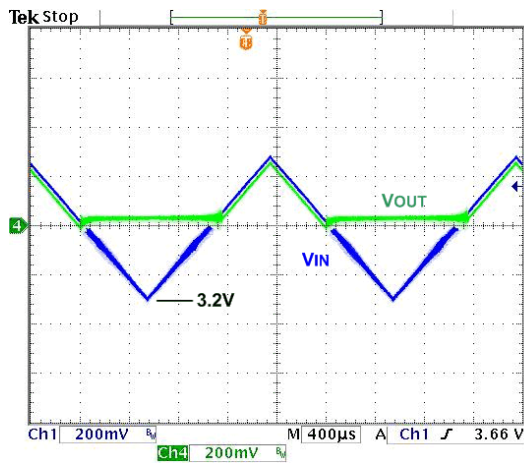


Figure 21. Bypass Entry / Exit, Slow  $V_{IN}$  Ramp 1 ms Edge, 500 mA Load, 3.2–3.8  $V_{IN}$

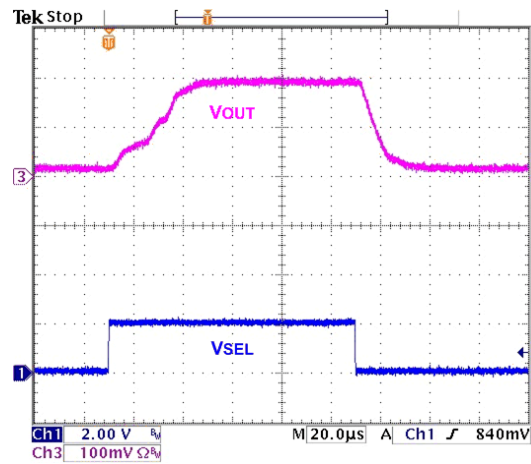


Figure 22.  $V_{SEL}$  Step,  $V_{IN} = 3.0\text{ V}$ , 500 mA Load



CIRCUIT DESCRIPTION

FAN48632 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low  $V_{IN}$  voltages. The regulator includes a Bypass Mode that activates when  $V_{IN}$  is above the boost regulator’s set point.

In anticipation of a heavy load transition, the set point can be adjusted upward by fixed amounts with the VSEL pin to reduce the required system headroom during lighter-load operation to save power.

Table 8. OPERATING STATES

Mode	Description	Invoked When
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Boost Soft-Start	$V_{OUT} < V_{OUT(MIN)}$
BST	Boost Operating Mode	$V_{OUT} = V_{OUT(MIN)}$
BPS	Bypass Mode	$V_{IN} > V_{OUT(MIN)}$

Boost Mode

The FAN48632 uses a current-mode modulator to achieve excellent transient response and smooth transitions between CCM and Discontinuous Conduction Mode (DCM) operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In light-load operation (DCM), frequency is reduced to maintain high efficiency.

Table 9. BOOST STARTUP SEQUENCE

Start State	Entry	Exit	End State	Timeout (μs)
LIN1	$V_{IN} > UVLO$ , EN = 1	$V_{OUT} > V_{IN}-300\text{ mV}$	SS	
			LIN2	512
LIN2	LIN1 Exit	$V_{OUT} > V_{IN}-300\text{ mV}$	SS	
		TIMEOUT	FAULT	1024
SS	LIN1 or LIN2 Exit	$V_{OUT} = V_{OUT(MIN)}$	BST	
		OVERLOAD TIMEOUT	FAULT	64

Shutdown and Startup

If EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, current flow is prevented from  $V_{IN}$  to  $V_{OUT}$ , as well as reverse flow from  $V_{OUT}$  to  $V_{IN}$ . During startup, it is recommended to keep DC current draw below 500 mA.

LIN State

When EN is HIGH and  $V_{IN} > UVLO$ , the regulator attempts to bring  $V_{OUT}$  within 300 mV of  $V_{IN}$  using the internal fixed current source from  $V_{IN}$  (Q3). The current is limited to LIN1 set point.

If  $V_{OUT}$  reaches  $V_{IN}-300\text{ mV}$  during LIN1 Mode, the SS state is initiated. Otherwise, LIN1 times out after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to 2 A. If  $V_{OUT}$  fails to reach  $V_{IN}-300\text{ mV}$  after 1024 μs, a fault condition is declared.

SS State

Upon the successful completion of the LIN state ( $V_{OUT} \geq V_{IN}-300\text{ mV}$ ), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS state,  $V_{OUT}$  is ramped up by stepping the internal reference. If  $V_{OUT}$  fails to reach regulation during the SS ramp sequence for more than 64 μs, a fault condition is declared. If large  $C_{OUT}$  is used, the reference is automatically stepped slower to avoid excessive input current draw.

BST State

This is a normal operating state of the regulator.

BPS State

If  $V_{IN}$  is above  $V_{REG}$  when the SS Mode successfully completes, the device transitions directly to BPS Mode.

Table 10. EN AND BYP LOGIC TABLE

EN	BYP	Mode	$V_{OUT}$
0	0	Shutdown	0
	1	Shutdown	0
1	0	Forced Bypass	$V_{IN}$
	1	Auto Bypass	$V_{REG}$ or $V_{IN}$ (if $V_{IN} > V_{REG}$ )

FAULT State

The regulator enters the FAULT state under any of the following conditions:

- $V_{OUT}$  fails to achieve the voltage required to advance from LIN state to SS state.
- $V_{OUT}$  fails to achieve the voltage required to advance from SS state to BST state.
- Boost current limit triggers for 2 ms during the BST state.
- $V_{DS}$  protection threshold is exceeded during BPS state.

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between  $V_{IN}$  and  $V_{OUT}$ . After waiting 20 ms, a restart is attempted.

Power Good

Power good is 0 FAULT, 1 POWER GOOD, open-drain input.

The Power good pin is provided for signaling the system when the regulator has successfully completed soft-start and no faults have occurred. Power good also functions as an early warning flag for high die temperature and overload conditions.

- PG is released HIGH when the soft-start sequence is successfully completed.
- PG is pulled LOW when PMOS current limit has triggered for 64  $\mu\text{s}$  OR the die the temperature exceeds 120°C. PG is re-asserted when the device cools below to 100°C.
- Any FAULT condition causes PG to be de-asserted.

**Over-Temperature**

The regulator shuts down when the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

**Bypass Operation**

In normal operation, the device automatically transitions from Boost Mode to Bypass Mode, if  $V_{IN}$  goes above target  $V_{OUT}$ . In Bypass Mode, the device fully enhances both Q1 and Q3 to provide a very low impedance path from  $V_{IN}$  to  $V_{OUT}$ . Entry to the Bypass Mode is triggered by condition where  $V_{IN} > V_{OUT}$  and no switching has occurred during past 5  $\mu\text{s}$ . To soften the entry to Bypass Mode, Q3 is driven as a linear current source for the first 5  $\mu\text{s}$ . Bypass Mode exit is triggered when  $V_{OUT}$  reaches the target  $V_{OUT}$  voltage. During Automatic Bypass Mode, the device is short-circuit protected by voltage comparator tracking the voltage drop from  $V_{IN}$  to  $V_{OUT}$ ; if the drop exceeds 200 mV, FAULT is declared.

With sufficient load to enforce CCM operation, the Bypass Mode to Boost Mode transition occurs at the target  $V_{OUT}$ . The corresponding input voltage at the transition point is:

$$V_{IN} \leq V_{OUT} + I_{LOAD} \cdot (DCR_L + R_{DS(ON)P}) \parallel R_{DS(ON)BYP} \quad (\text{eq. 1})$$

The Bypass Mode entry threshold has 25 mV hysteresis imposed at  $V_{OUT}$  to prevent cycling between modes. The transition from Boost Mode to Bypass Mode occurs at the target  $V_{OUT} + 25 \text{ mV}$ . The corresponding input voltage is:

$$V_{IN} \geq V_{OUT} + 25\text{mV} + I_{LOAD} \cdot (DCR_L + R_{DS(ON)P}) \quad (\text{eq. 2})$$

**Forced Bypass**

Entry to Forced Bypass Mode initiates with a current limit on Q3 and then proceeds to a true bypass state. To prevent reverse current to the battery, the device waits until output discharges below  $V_{IN}$  before entering Forced Bypass Mode.

Low- $I_Q$  Forced Bypass Mode is available for the FAN48632. After the transition is complete, most of the internal circuitry is disabled to minimize quiescent current draw. OCP, UVLO, output OVP and over-temperature protections are inactive in Forced Bypass Mode.

In Forced Bypass Mode,  $V_{OUT}$  can follow  $V_{IN}$  below  $V_{OUT(MIN)}$ .

**VSEL**

$V_{SEL}$  can be asserted in anticipation of a positive load transient. Raising  $V_{SEL}$  increases  $V_{OUT(MIN)}$  by a fixed amount and  $V_{OUT}$  is stepped to the corresponding target output voltage in 20  $\mu\text{s}$ . The functionality can also be utilized to mitigate undershoot during severe line transients, while minimizing  $V_{OUT}$  during more benign operating conditions to save power.

APPLICATION INFORMATION

Output Capacitance (C<sub>OUT</sub>)

Stability

The effective capacitance (C<sub>EFF</sub>) of small, high-value, ceramic capacitors decreases as bias voltage increases. FAN48632 is guaranteed for stable operation with the minimum value of C<sub>EFF</sub> (C<sub>EFF(MIN)</sub>) of 14 μF.

Inductor Selection

The recommended nominal inductance value is 0.47 μH.

FAN48632 employs valley-current limiting; peak inductor current can exceed 4.4 A for a short duration during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading as only valley of the inductor current ripple is controlled.

Startup

Input current limiting is in effect during soft-start, which limits the current available to charge C<sub>OUT</sub> and any additional capacitance on the V<sub>OUT</sub> line. If the output fails to achieve regulation within the limits described in the Startup section, a FAULT occurs, causing the circuit to shut down then restart after a significant time period. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high-current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempts soft-start, only to have the output capacitance discharged by the load when in a FAULT state.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C<sub>OUT</sub>. During t<sub>ON</sub>, when the boost switch is on, all load current is supplied by C<sub>OUT</sub>. Output ripple is calculated as:

$$V_{\text{RIPPLE(P-P)}} = t_{\text{ON}} \cdot \frac{I_{\text{LOAD}}}{C_{\text{OUT}}} \quad (\text{eq. 3})$$

and

$$t_{\text{ON}} = t_{\text{SW}} \cdot D = t_{\text{SW}} \cdot \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \quad (\text{eq. 4})$$

therefore:

$$V_{\text{RIPPLE(P-P)}} = t_{\text{SW}} \cdot \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \cdot \frac{I_{\text{LOAD}}}{C_{\text{OUT}}} \quad (\text{eq. 5})$$

and

$$t_{\text{SW}} = \frac{1}{f_{\text{SW}}} \quad (\text{eq. 6})$$

As can be seen from eq. 5, the maximum V<sub>RI</sub>PPLE occurs when V<sub>IN</sub> is at minimum and I<sub>LOAD</sub> is at maximum.

2.0 A Pulsed Loads for GSM Applications

The FAN48632 can support 2 A load pulses for GSM and GSM Edge applications, according to the minimum V<sub>IN</sub> levels shown in Figure 23.

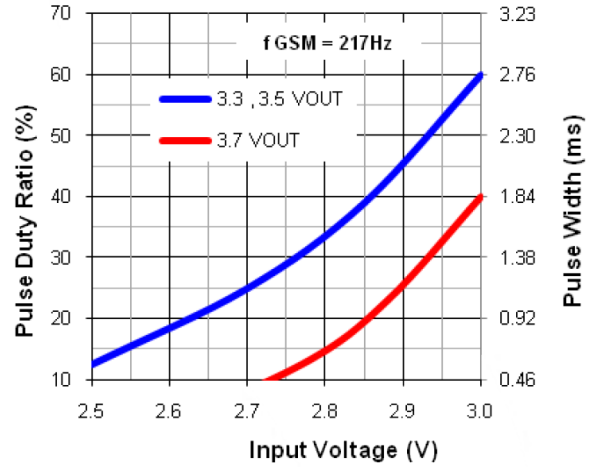


Figure 23. Minimum V<sub>IN</sub> for 2 A GSM Pulse, 3.5 V<sub>OUT</sub>

Results shown use circuit/components of Figure 1 with device mounted on standard evaluation platform (layout Figure 24).

Layout Recommendation

To minimize spikes at V<sub>OUT</sub>, C<sub>OUT</sub> must be placed as close as possible to PGND and V<sub>OUT</sub>, as shown in Figure 24. The associated PGND and V<sub>OUT</sub> routes are best made directly on the top copper layer, rather than thru vias.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

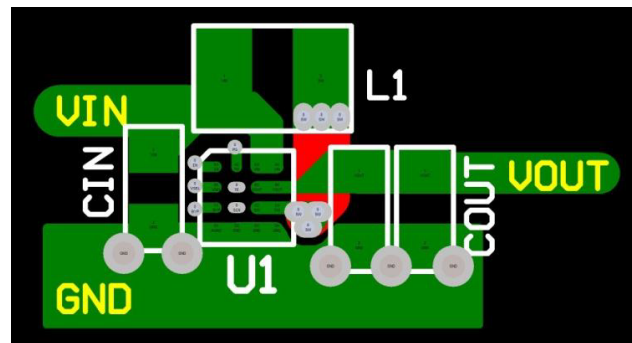


Figure 24. Layout Recommendation

# FAN48632

**Table 11. PRODUCT-SPECIFIC DIMENSIONS**

D	E	X	Y
1.780 ±0.030	1.780 ±0.030	0.290	0.290

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

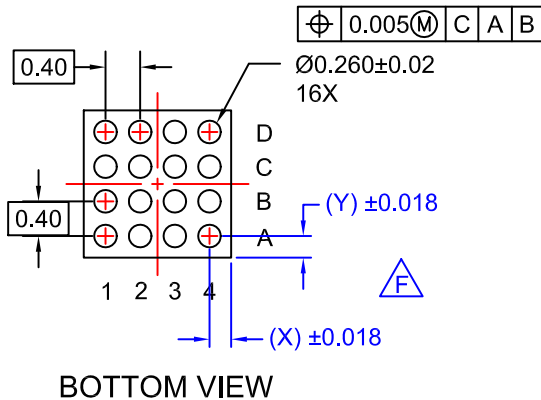
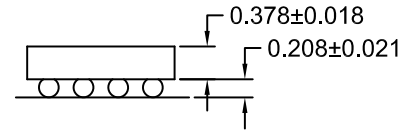
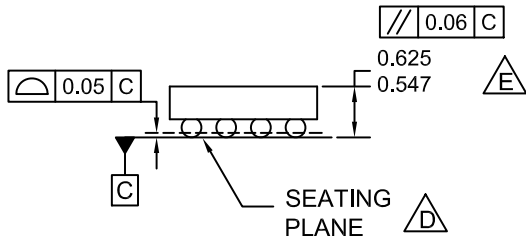
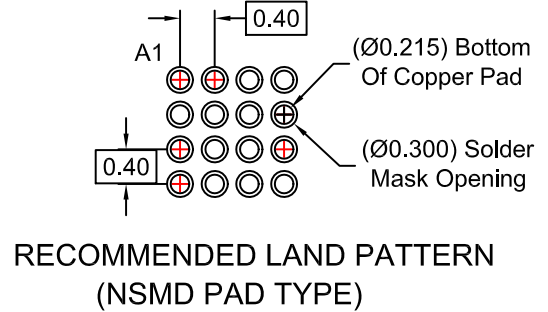
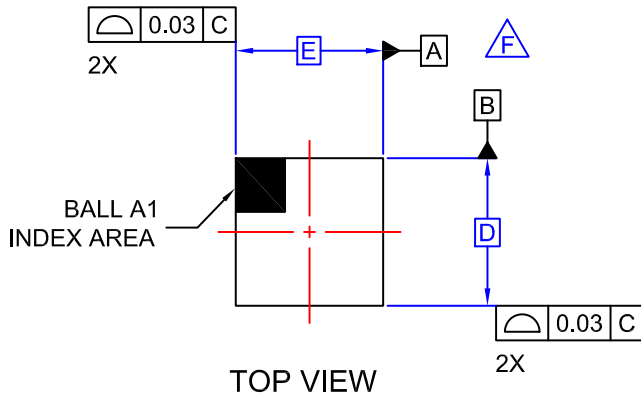
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### WLCSP16 1.78x1.78x0.586

CASE 567SY  
ISSUE O

DATE 30 NOV 2016



#### NOTES

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS  $586 \pm 39$  MICRONS (547-625 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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