TPS2052C, TPS2062C, TPS2062C-2, TPS2066C, TPS2066C-2
TPS2060C, TPS2064C, TPS2064C-2, TPS2002C, TPS2003C
SLVSAX6H – OCTOBER 2011 – REVISED DECEMBER 2015

TPS20xxC, TPS20xxC-2 Dual Channel, Current-Limited, Power-Distribution Switches

1 Features

- Dual Power Switch Family
- Rated Currents of 0.5 A, 1 A, 1.5 A, 2 A
- Accurate ±20% Current Limit Tolerance
- Fast Overcurrent Response – 2 µs (Typical)
- 70-mΩ (Typical) High-Side N-Channel MOSFET
- Operating Range: 4.5 V to 5.5 V
- Deglitched Fault Reporting ($\overline{\text{FLTx}}$)
- Selected Parts With (TPS20xxC) and Without (TPS20xxC-2) Output Discharge
- Reverse Current Blocking
- Built-in Softstart
- Pin for Pin With Existing *TI Switch Portfolio*
- Ambient Temperature Range: –40°C to 85°C

2 Applications

- USB Ports or Hubs, Laptops, Desktops
- High-Definition Digital TVs
- Set Top Boxes
- Short Circuit Protection

3 Description

The TPS20xxC and TPS20xxC-2 dual power-distribution switch family is intended for applications such as USB where heavy capacitive loads and short-circuits may be encountered. This family offers multiple devices with fixed current-limit thresholds for applications between 0.5 A and 2 A.

The TPS20xxC and TPS20xxC-2 dual family limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the current-limit threshold. This provides a predictable fault current under all conditions. The fast overcurrent response time eases the burden on the main 5 V supply to provide regulated power when the output is shorted. The power-switch rise and fall times are controlled to minimize current surges during turnon and turnoff.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2052C TPS2062C TPS2066C TPS2066C-2 TPS2060C TPS2064C TPS2064C-2	MSOP (8)	3.00 mm × 3.00 mm
TPS2062C TPS2066C	SOIC (8)	3.90 mm × 4.90 mm
TPS2062C-2	SON (8)	3.00 mm × 3.00 mm
TPS2002C TPS2003C	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

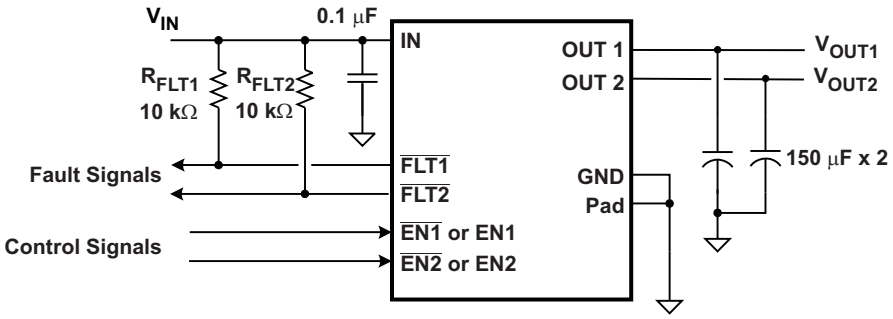


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2013) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision F (November 2012) to Revision G — **Page**

- Changed device TPS2062C-2 SON-8 packages From: Preview To: Active. ... 4
- Changed devices TPS2066C-2, and TPS2064C-2 MSOP-8 package From: Preview To: Active ... 4

Changes from Revision E (August 2012) to Revision F — **Page**

- Changed Feature from: Rated Currents of 1 A, 1.5 A, 2 A to: Rated Currents of 0.5 A, 1 A, 1.5 A, 2 A ... 1
- Changed Feature from: Output Discharge When Disabled to: Selected parts with (TPS20xxC) and without (TPS20xxC-2) Output Discharge ... 1
- Added TPS2052C, TPS2062C-2, TPS2064C-2, and TPS2066C-2 devices to Table 1 ... 4
- Added TPS2052C, TPS2062C-2, TPS2064C-2, and TPS2066C-2 devices to Table 2 ... 4
- Added TPS2052C, TPS2062C-2, TPS2064C-2, and TPS2066C-2 devices to RECOMMENDED OPERATING CONDITIONS table ... 6
- Added TPS2052C and TPS2066C-2 devices to $r_{DS(on)}$ ... 8
- Added the TPS2052C and TPS2064C-2 devices to I_{OS} ... 8
- Added Leakage current to Electrical Characteristics table ... 8
- Added text to the SOFTSTART, REVERSE BLOCKING AND DISCHARGE OUTPUT section ... 18
- Added last paragraph in the DISCHARGE OUTPUT section ... 18

Changes from Revision D (July 2012) to Revision E **Page**

- Changed devices TPS2002C and TPS2003C SON-10 package From: Preview To: Active 4
- Changed the I_{OS} current limit values for TPS2002C and 03C (2 A) 8
- Corrected Note 2 reference in the Electrical Characteristics table 9

Changes from Revision C (June 2012) to Revision D **Page**

- Changed the Device Information table, Package Devices and Marking columns 4

Changes from Revision B (March 2012) to Revision C **Page**

- Changed devices TPS2062C and TPS2066C SOIC-8 package From: Preview To: Active 4
- Changed the TPS2062C and 66C $r_{DS(on)}$ D package TYP value From: 84 to 90 mΩ 8

Changes from Revision A (March 2012) to Revision B **Page**

- Changed device TPS2060C MSOP-8 package From: Preview To: Active 4

Changes from Original (October 2011) to Revision A **Page**

- Changed devices TPS2062C and TPS2066C MSOP-8 package From: Preview to Active 4
- Changed the I_{OS} current limit values for TPS2062C/66C (1 A) 8

5 Device Comparison Table

Table 1. Devices

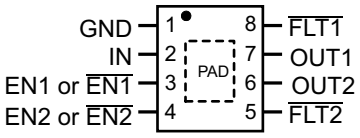
DEVICES	RATED CURRENT	STATUS			
		MSOP-8 (PowerPad™)	SOIC-8	SON-8	VSON-10
TPS2052C	0.5 A	Active	—	—	—
TPS2062C TPS2066C	1 A	Active and Active	Active and Active	—	—
TPS2062C-2 TPS2066C-2	1 A	— and Active	—	Active and —	—
TPS2060C TPS2064C	1.5 A	Active and Active	—	—	—
TPS2064C-2	1.5 A	Active	—	—	—
TPS2002C TPS2003C	2 A	—	—	—	Active and Active

Table 2. Device Information

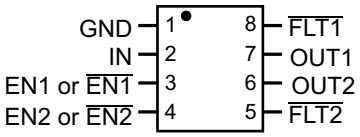
PART NUMBER	MAXIMUM OPERATING CURRENT	ENABLE	OUTPUT DISCHARGE
TPS2052C	0.5	High	Y
TPS2062C	1	Low	Y
TPS2062C-2	1	Low	N
TPS2066C	1	High	Y
TPS2066C-2	1	High	N
TPS2060C	1.5	Low	Y
TPS2064C	1.5	High	Y
TPS2064C-2	1.5	High	N
TPS2002C	2	Low	Y
TPS2003C	2	High	Y

6 Pin Configuration and Functions

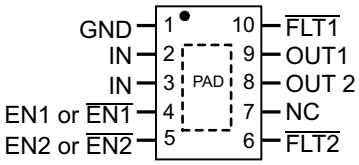
DGN Package
8-Pin MSOP
Top View



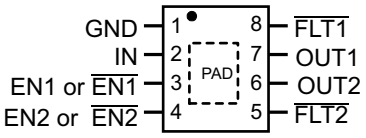
D Package
8-Pin SOIC
Top View



DRC Package
10-Pin VSON
Top View



DRB Package
8-Pin SON
Top View



Pin Functions

PIN					TYPE(1)	DESCRIPTION
NAME	MSOP	SOIC	VSON	SON		
GND	1	1	1	1	GND	Ground connection
IN	2	2	2, 3	2	I	Input voltage and power-switch drain; connect a 0.1 µF or greater ceramic capacitor from IN to GND close to the IC
EN1	3(2)	3(3)	4(4)	—	I	Enable input channel 1, logic high turns on power switch
	–(5)	–(6)	–(7)	—		
$\overline{EN1}$	–(2)	–(3)	–(4)	3	I	Enable input channel 1, logic low turns on power switch
	3(5)	3(6)	4(7)			
EN2	4(2)	4(3)	5(4)	—	I	Enable input channel 2, logic high turns on power switch
	–(5)	–(6)	–(7)	—		
$\overline{EN2}$	–(2)	–(3)	–(4)	4	I	Enable input channel 2, logic low turns on power switch
	4(5)	4(6)	5(7)			
$\overline{FLT2}$	5	5	6	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions on channel 2
NC	—	—	7	—	O	No connect – leave floating
OUT2	6	6	8	6	O	Power-switch output channel 2, connected to load
OUT1	7	7	9	7	O	Power-switch output channel 1, connected to load
$\overline{FLT1}$	8	8	10	8	O	Active-low open-drain output, asserted during over-current, or overtemperature conditions on channel 1
PowerPAD™	PAD	—	PAD	—	GND	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PAD to GND plane as a heatsink.

(1) I = Input, O = Output, GND = Ground
(2) Applies to TPS2052C, TPS2066C, TPS2066C-2, TPS2064C, and TPS2064C-2
(3) Applies to TPS2066C
(4) Applies to TPS2003C
(5) Applies to TPS2062C and TPS2060C
(6) Applies to TPS2062C
(7) Applies to TPS2002C

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Voltage range on IN, OUTx, ENx or $\overline{ENx}$, $\overline{FLTx}$(4)	–0.3	6	V
Voltage range from IN to OUT	–6	6	V
Maximum junction temperature, T_J	Internally limited		°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) All voltages are with respect to GND unless otherwise noted.
(4) See *Input and Output Capacitance*.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		IEC 61000-4-2, contact discharge(3)	±8000	V
		IEC 61000-4-2, air-gap discharge(3)	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) V_{OUT} was surged on a PCB with input and output bypassing per Figure 22 (except input capacitor was 22 µF) with no device failure.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN		4.5		5.5	V
V_{Enable}	Input voltage, ENx or $\overline{ENx}$		0		5.5	V
I_{OUTx}	Continuous output current, OUTx	TPS2052C			0.5	A
		TPS2062C, TPS2062C-2, TPS2066C, and TPS2066C-2			1	
		TPS2060C, TPS2064C, and TPS2064C-2			1.5	
		TPS2002C and TPS2003C			2	
T_J	Operating junction temperature		–40		125	°C
$I_{\overline{FLTx}}$	Sink current into $\overline{FLTx}$		0		5	mA

7.4 Thermal Information

THERMAL METRIC[1][2]		TPS2052C TPS2062C TPS2066C TPS2066C-2 TPS2060C TPS2064C TPS2064C-2	TPS2062C TPS2066C	TPS2062C-2	TPS2002C TPS2003C	UNIT
		DGN (MSOP)	D (SOIC)	DRB (SON)	DRC (VSON)	
		8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.2	129.9	50.8	45.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	110.5	83.5	60.3	58	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.7	70.4	26.3	21.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	36.6	2.1	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	66.9	26.5	21.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.3	n/a	9.8	9.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

7.5 Electrical Characteristics: $T_J = T_A = 25°C$

V_{IN} = 5 V, V_{ENx} = VIN or $V_{\overline{ENx}}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	On-resistance	TPS2052C (0.5 A)	DGN		70	84	mΩ
		TPS2052C (0.5 A) –40°C ≤ (T_J, T_A) ≤ 85°C	DGN		70	95	
		TPS2062C, 66C, and 66C-2 (1 A)	DGN		70	84	
		TPS2062C, 66C, and 66C-2 (1 A), –40°C ≤ (T_J, T_A) ≤ 85°C	DGN		70	95	
		TPS2062C and 66C (1 A)	D		90	108	
		TPS2062C and 66C (1 A) –40°C ≤ (T_J, T_A) ≤ 85°C	D		90	122	
		TPS2062C-2 (1 A)	DRB		73	87	
		TPS2062C-2 (1 A) –40°C ≤ (T_J, T_A) ≤ 85°C	DRB		73	101	
		TPS2060C, 64C, and 64C-2 (1.5 A)			70	84	
		TPS2060C, 64C, and 64C-2 (1.5 A) –40°C ≤ (T_J, T_A) ≤ 85°C			70	95	
		TPS2002C and 03C (2 A)			70	84	
		TPS2002C and 03C (2 A) –40°C ≤ (T_J, T_A) ≤ 85°C			70	95	
CURRENT LIMIT							
I_{OS}	Current-limit (see Figure 28)	TPS2052C (0.5 A)		0.75	1	1.25	A
		TPS2062C, 62C-2, 66C, and 66C-2 (1 A)		1.28	1.61	1.94	
		TPS2060C, 64C, and 64C-2 (1.5 A)		1.83	2.29	2.75	
		TPS2002C and 03C (2 A)		2.55	3.15	3.77	
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	$I_{(OUTx)}$ = 0 mA			0.01	1	µA
I_{S1E}	Supply current, single switch enabled	$I_{(OUTx)}$ = 0 mA			60	75	
I_{S2E}	Supply current, both switches enabled	$I_{(OUTx)}$ = 0 mA			100	120	
I_{LKG}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5.5 V, disabled, measured I_{VIN}	TPS20xxC-2		0.05	1	
	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measured $I_{(OUTx)}$			0.15	1	

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature

Electrical Characteristics: $T_J = T_A = 25°C$ (continued)

V_{IN} = 5 V, V_{ENx} = VIN or $V_{\overline{ENx}}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance(2)	V_{IN} = V_{OUTx} = 5 V, disabled	TPS20xxC	400	470	600	Ω

(2) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.6 Electrical Characteristics: –40°C ≤ ($T_J = T_A$) ≤ 125°C(1)

4.5 V ≤ V_{IN} ≤ 5.5 V, V_{ENx} = V_{IN} or $V_{\overline{ENx}}$ = 0 V, I_{OUTx} = 0 A (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	On-resistance	TPS2052C (0.5 A)	DGN		70	112	mΩ
		TPS2062C, 66C, and 66C-2 (1 A)	DGN		70	112	
		TPS2062C and 66C (1 A)	D		90	135	
		TPS2062C-2 (1 A)	DRB		73	115	
		TPS2060C, 64C, and 64C-2 (1.5 A)	DGN		70	112	
		TPS2002C and 03C (2 A)	DRC		70	112	
ENABLE INPUT (ENx or $\overline{ENx}$)							
V_{IH}	ENx ($\overline{ENx}$), High-level input voltage	4.5 V ≤ V_{IN} ≤ 5.5 V		2			V
V_{IL}	ENx ($\overline{ENx}$), Low-level input Voltage					0.8	
	Hysteresis	V_{IN} = 5 V			0.14		
	Leakage current	V_{ENx} = 5.5 V or 0 V, $V_{\overline{ENx}}$ = 0 V or 5.5 V		–1	0	1	µA
t_{on}	Turnon time (3)	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, ENx ↑ or $\overline{ENx}$ ↓ (see Figure 25, Figure 26, and Figure 23) 1 A, 1.5 A, 2 A Rated		1.4	1.9	2.4	ms
t_{off}	Turnoff time (3)	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, ENx ↑ or $\overline{EN}$ ↓ (see Figure 25, Figure 26, and Figure 23) 1 A, 1.5 A, 2 A Rated		1.95	2.60	3.25	ms
t_r	Rise time, output (3)	C_L = 1 µF, R_L = 100 Ω (see Figure 24) 1 A, 1.5 A, 2 A Rated		0.58	0.82	1.15	ms
t_f	Fall time, output (3)	C_L = 1 µF, R_L = 100 Ω (see Figure 24) 1 A, 1.5 A, 2 A Rated		0.33	0.47	0.66	ms
CURRENT LIMIT							
I_{OS}	Current-limit (see Figure 28)	TPS2052C (0.5 A)		0.7	1	1.3	A
		TPS2062C, 62C-2, 66C, and 66C-2 (1 A)		1.12	1.61	2.10	
		TPS2060C, 64C, and 64C-2 (1.5 A)		1.72	2.29	2.86	
		TPS2002C and 03C (2 A)		2.35	3.15	3.95	
t_{IOS}	Short-circuit response time	V_{IN} = 5 V (see Figure 27), One-half full load → $R_{(SHORT)}$ = 50 mΩ, Measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	Standard conditions, $I_{(OUTx)}$ = 0 mA			0.01	10	µA
I_{S1E}	Supply current, single switch enabled	Standard conditions, $I_{(OUTx)}$ = 0 mA				90	
I_{S2E}	Supply current, both switches enabled	Standard conditions, $I_{(OUTx)}$ = 0 mA				150	
I_{LKG}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5.5 V, disabled, measured I_{VIN}	TPS20xxC-2		0.05		
	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measured $I_{(OUTx)}$			0.20		
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	VIN rising		3.4		4.0	V
	Hysteresis, IN				0.14		V

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature.
(2) Typical values are at 5 V and 25°C.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

Electrical Characteristics: –40°C ≤ (T_J = T_A) ≤ 125°C[1] (continued)

4.5 V ≤ V_{IN} ≤ 5.5 V, V_{ENx} = V_{IN} or $V_{\overline{ENx}}$ = 0 V, I_{OUTx} = 0 A (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
$\overline{FLTx}$						
Output low voltage, $\overline{FLTx}$	$I_{(\overline{FLTx})}$ = 1 mA				0.2	V
Off-state leakage	$V_{(\overline{FLTx})}$ = 5.5 V				1	µA
$\overline{FLTx}$ deglitch [3]	$\overline{FLTx}$ overcurrent assertion and deassertion		7	10	13	ms
OUTPUT DISCHARGE						
Output pulldown resistance[3]	V_{IN} = 5 V, V_{OUT} = 5 V, disabled	TPS20xxC	300	470	800	Ω
	V_{IN} = 4 V, V_{OUT} = 5 V, disabled	TPS20xxC	350	560	1200	
THERMAL SHUTDOWN						
Junction thermal shutdown threshold	In current limit		135			°C
	Not in current limit		155			
Hysteresis				20		°C

7.7 Typical Characteristics

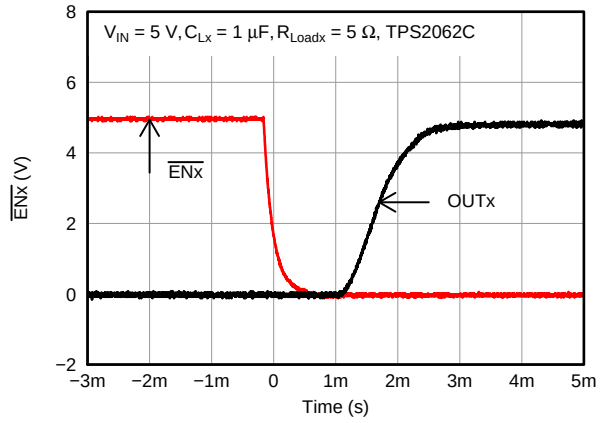


Figure 1. TPS2062C Turnon Delay and Rise Time With 1-µF Load

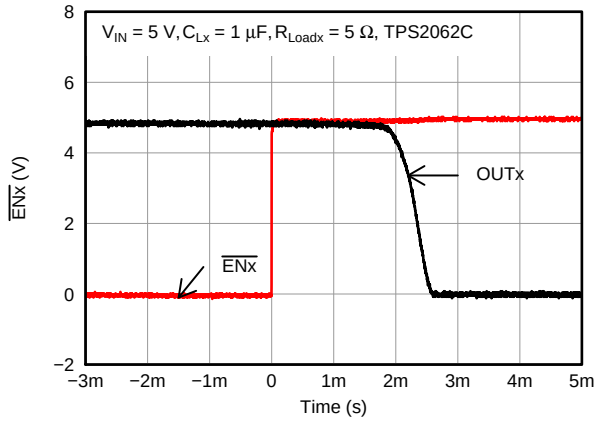


Figure 2. TPS2062C Turnoff Delay and Fall Time With 1-µF Load

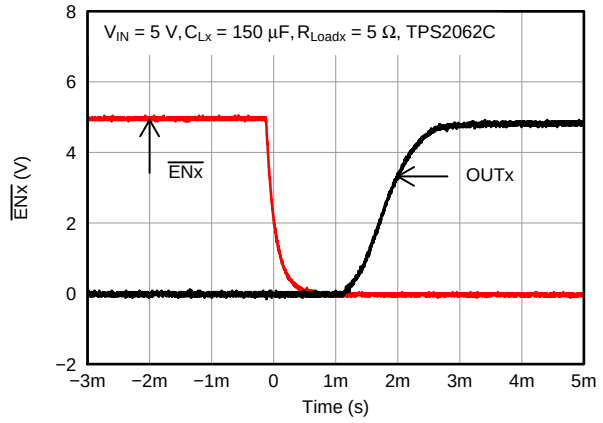


Figure 3. TPS2062C Turnon Delay and Rise Time With 150-µF Load

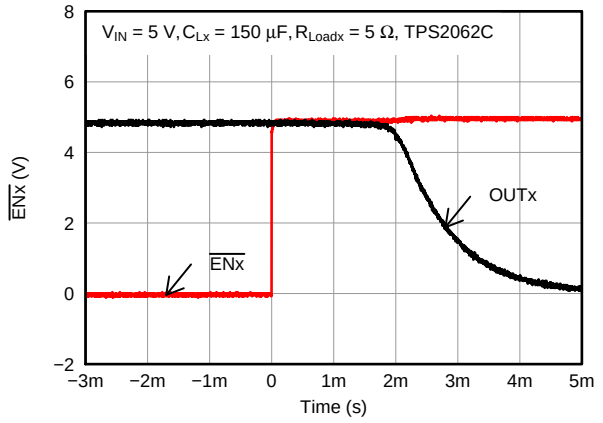


Figure 4. TPS2062C Turnoff Delay and Fall Time With 150-µF Load

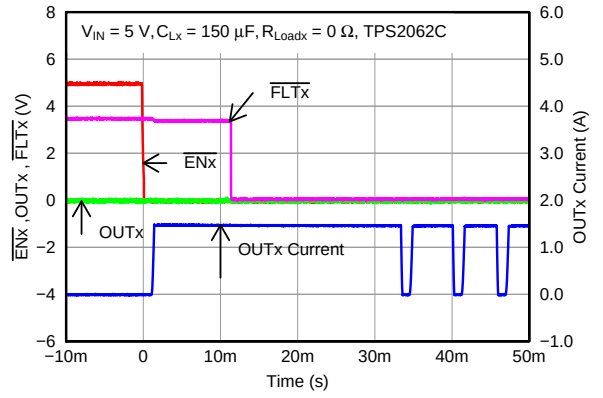


Figure 5. TPS2062C Enable Into Short

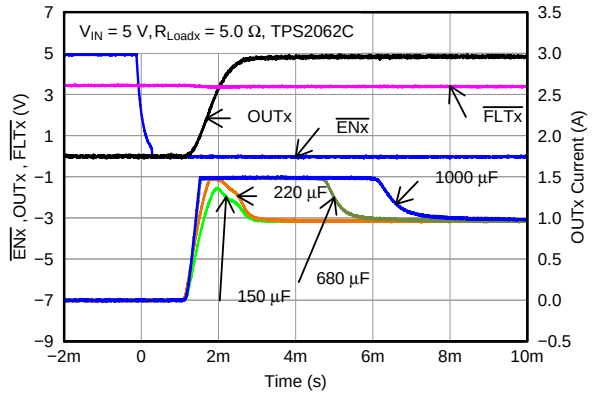


Figure 6. TPS2062C In-rush Current With Different Load Capacitance

Typical Characteristics (continued)

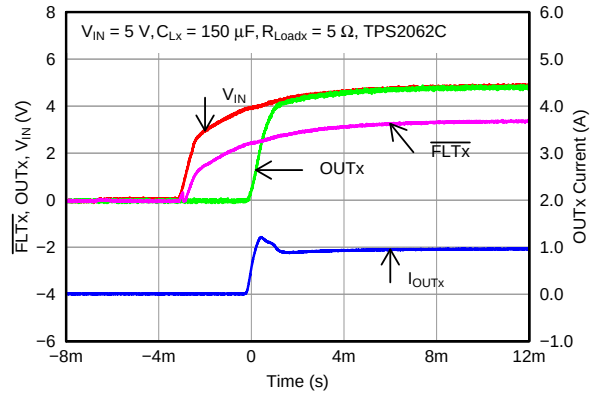


Figure 7. TPS2062C Power Up – Enabled

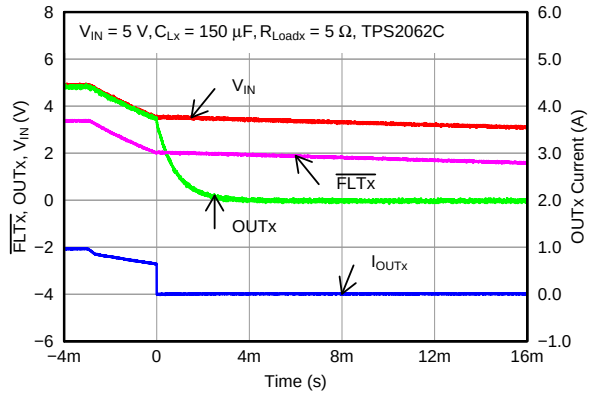


Figure 8. TPS2062C Power Down – Enabled

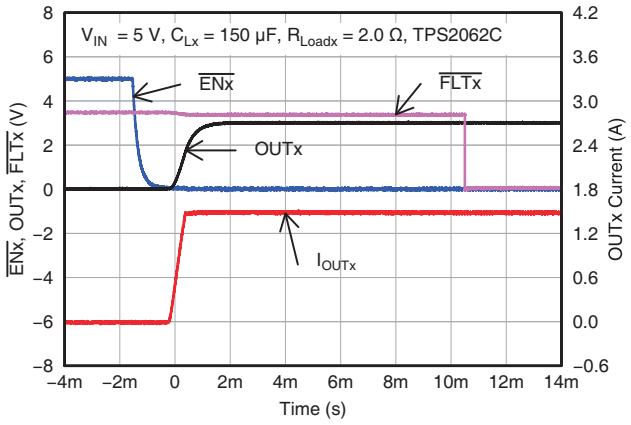


Figure 9. TPS2062C Enable With 2-Ω Load

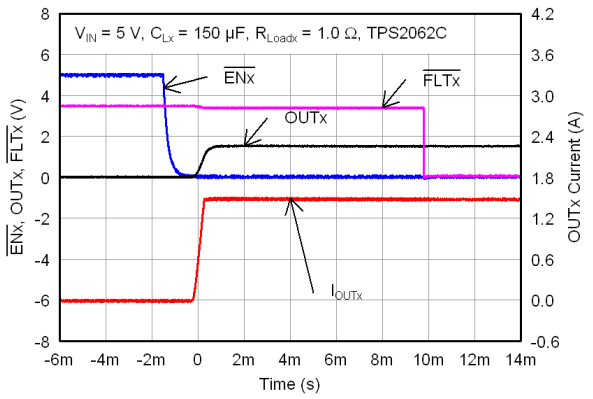


Figure 10. TPS2062C Enable With 1-Ω Load

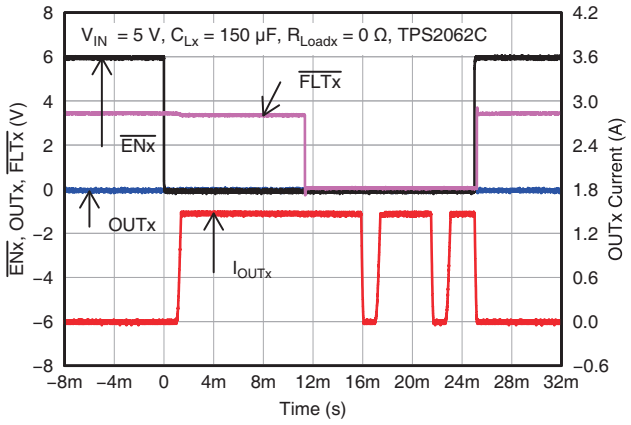


Figure 11. TPS2062C Enable and Disable into Output Short

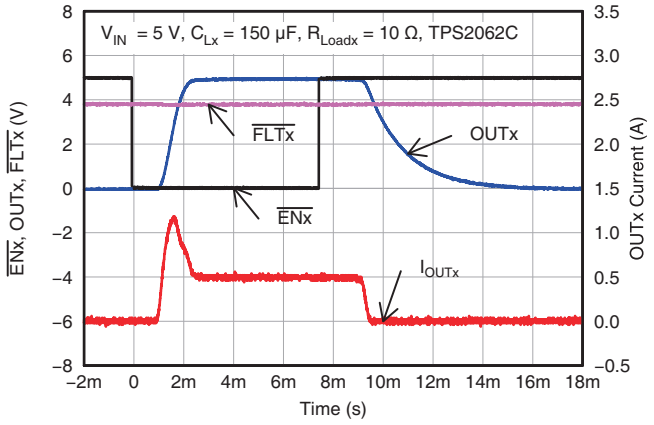


Figure 12. TPS2062C Enable and Disable into 10-Ω Load

Typical Characteristics (continued)

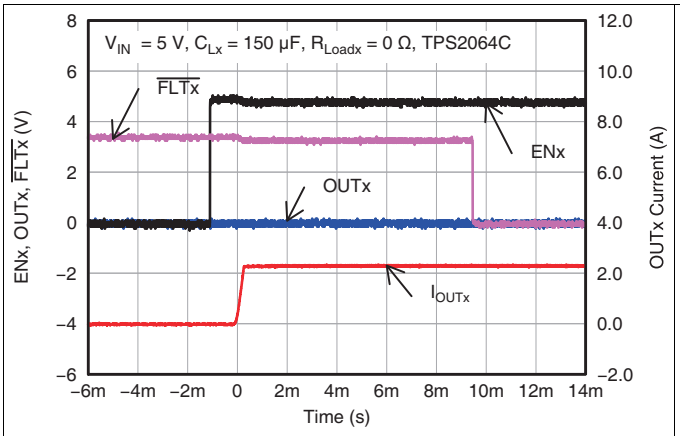


Figure 13. TPS2064C Enable into Short

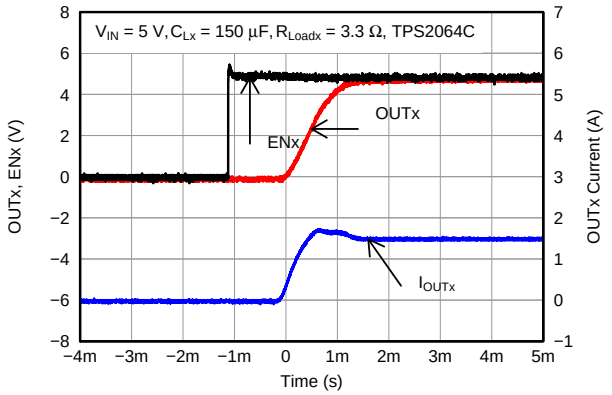


Figure 14. TPS2064C Enable into 3.3 Ω and 150-µF Laod

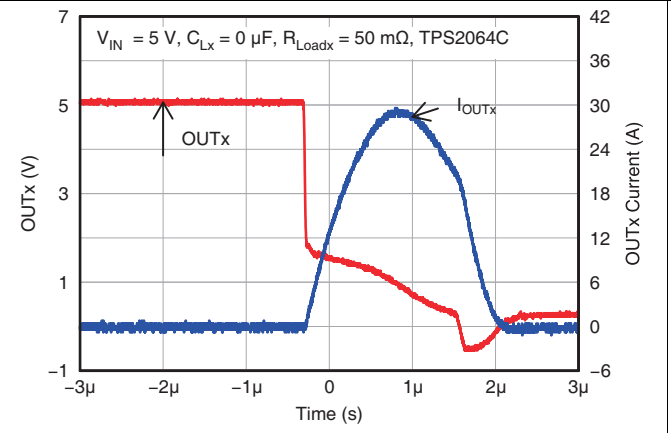


Figure 15. TPS2064C Short Applied

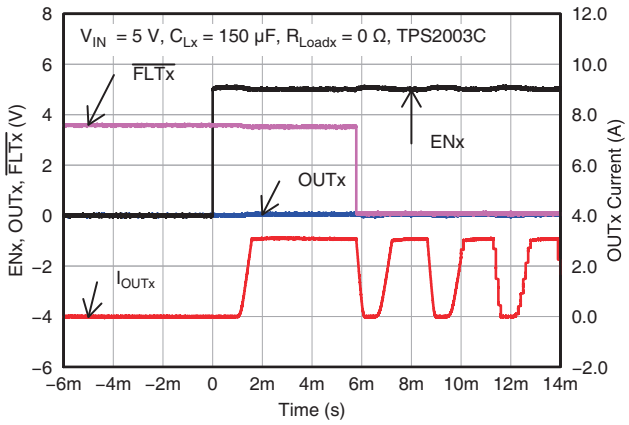


Figure 16. TPS2003C Enable into Short

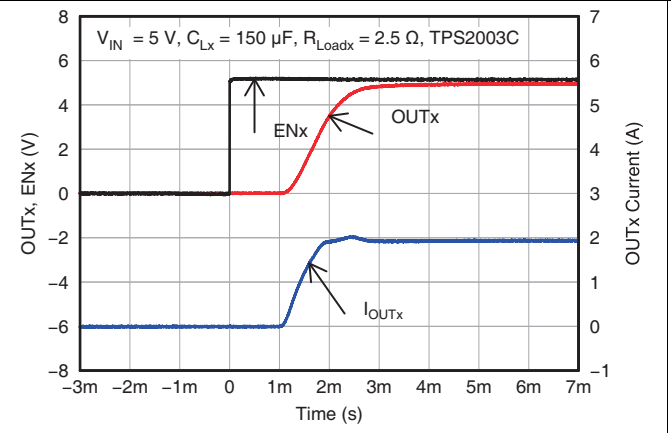


Figure 17. TPS2003C Enable into 2.5 Ω and 150-µF Load

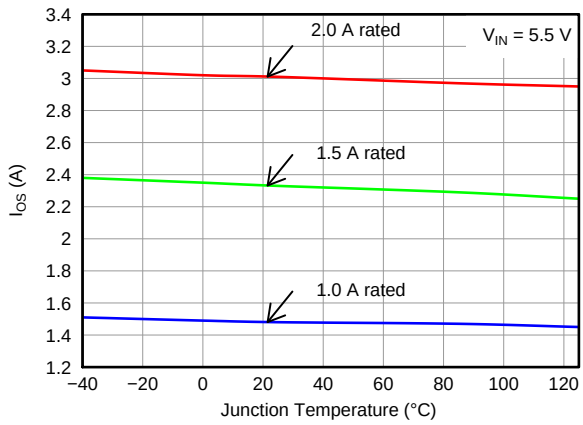


Figure 18. Current Limit (I_{OS}) vs Temperature

Typical Characteristics (continued)

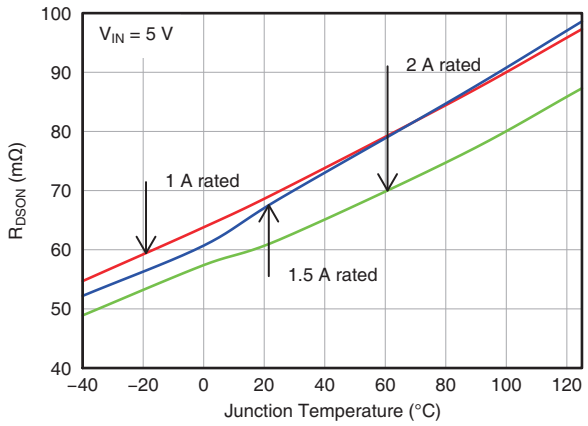


Figure 19. Input - output Resistance ($R_{DS(ON)}$) vs Temperature

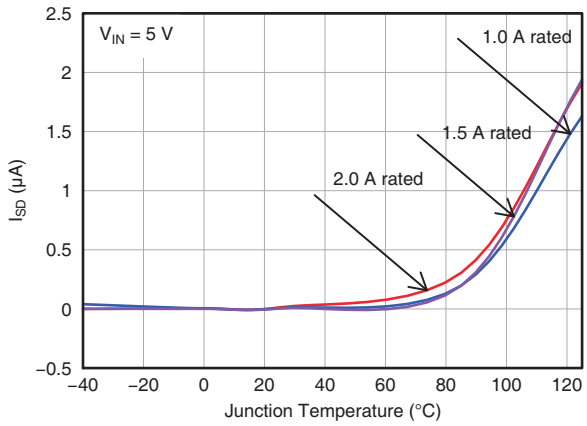


Figure 20. Supply Current (Device Disable) - I_{SD} vs Temperature

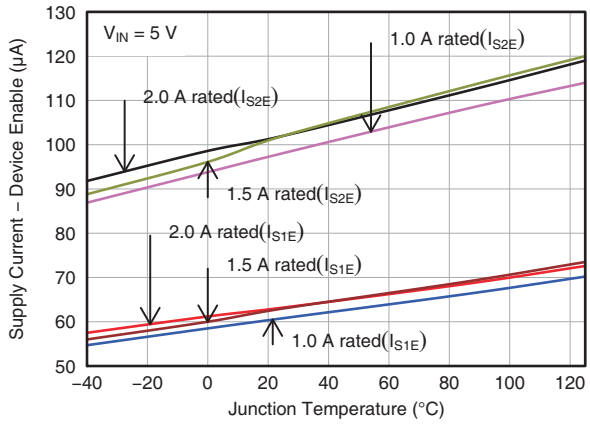


Figure 21. Supply Current (Enable) - I_{SE} vs Temperature

8 Parameter Measurement Information

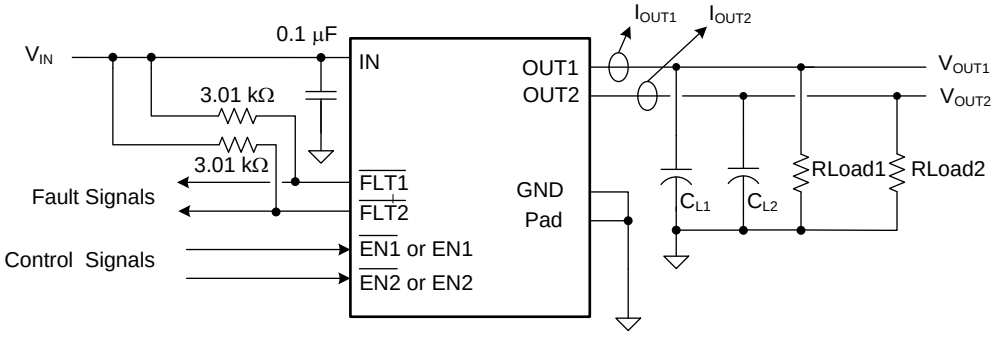


Figure 22. Test Circuit for System Operation for the Typical Characteristics

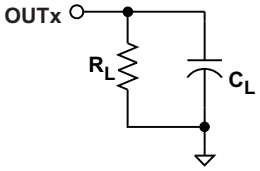


Figure 23. Output Rise / Fall Test Load

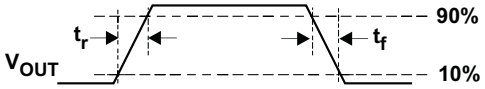


Figure 24. Power-On and Off Timing

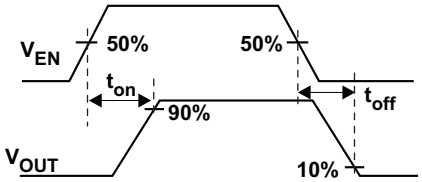


Figure 25. Enable Timing, Active High Enable

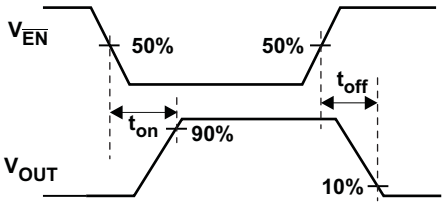


Figure 26. Enable Timing, Active Low Enable

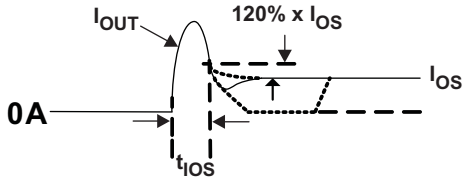


Figure 27. Output Short Circuit Parameters

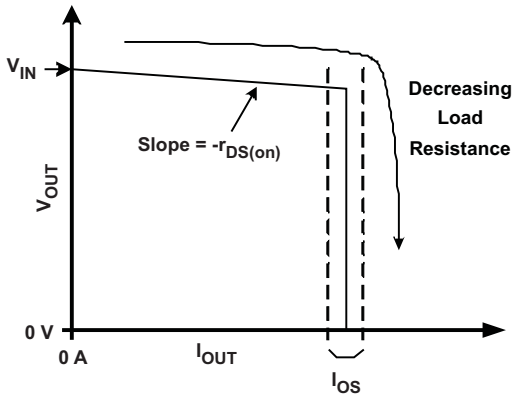


Figure 28. Output Characteristic Showing Current Limit

9 Detailed Description

9.1 Overview

The TPS20xxC and TPS20xxC-2 are dual current-limited, power-distribution switches providing between 0.5 A and 2 A of continuous load current in 5-V circuits. These parts use N-channel MOSFETs for low resistance, maintaining output voltage load regulation. They are designed for applications where short circuits or heavy capacitive loads are encountered. Device features include UVLO, ON/OFF control (Enable), reverse blocking when disabled, output discharge when TPS20xxC disabled, overcurrent protection, overtemperature protection, and deglitched fault reporting. They are pin for pin with existing TI Switch Portfolio.

9.2 Functional Block Diagram

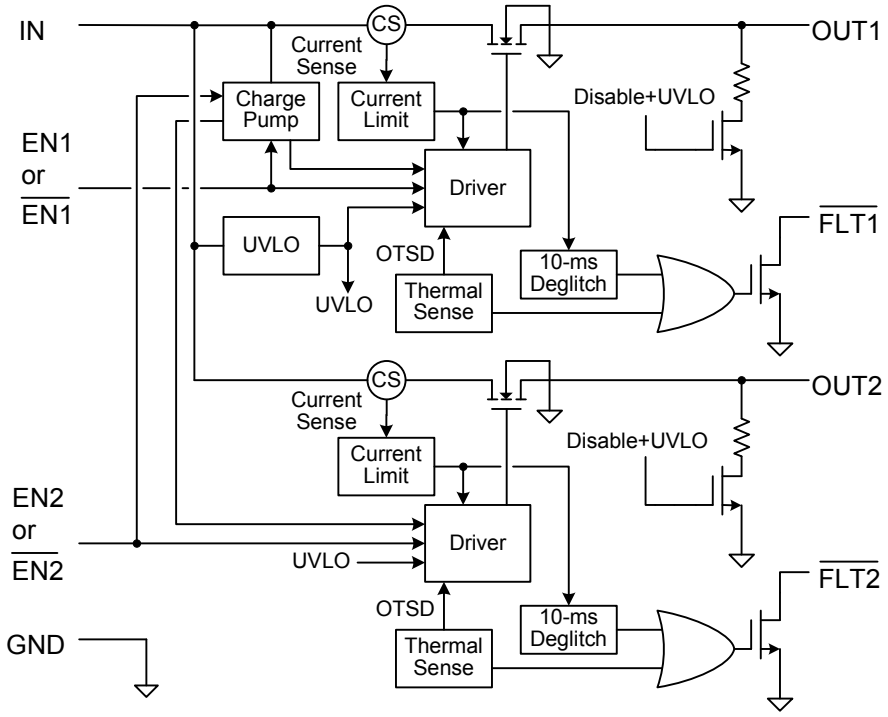


Figure 29. TPS20xxC Functional Block Diagram

Functional Block Diagram (continued)

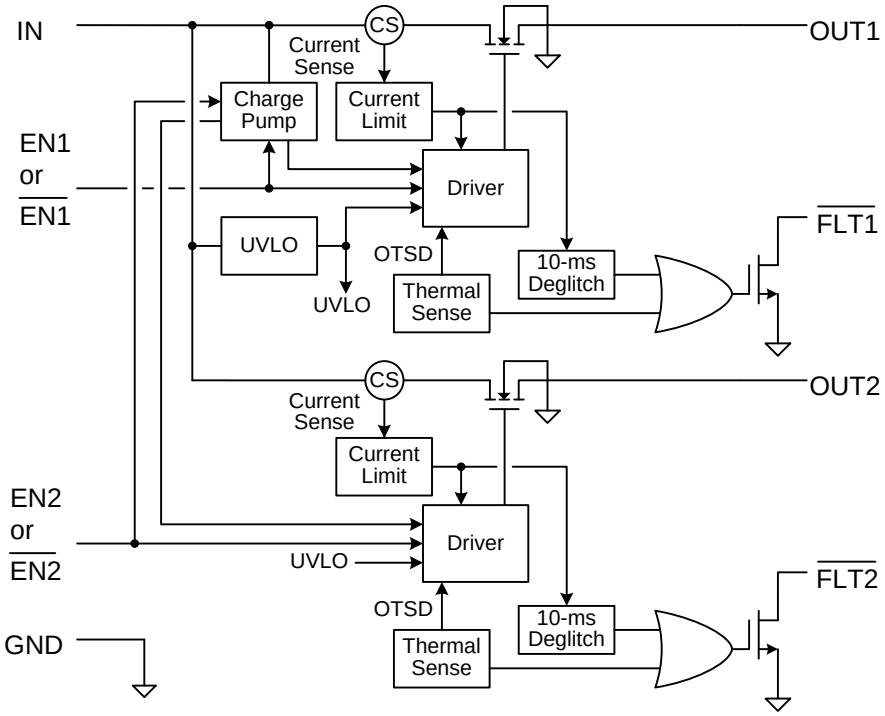


Figure 30. TPS20xxC-2 Functional Block Diagram

9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch when the input voltage is below the UVLO threshold. Built-in hysteresis prevents unwanted ON/OFF cycling due to input voltage drop from large current surges. $\overline{FLTx}$ is high impedance when the TPS20xxC and TPS20xxC-2 dual are in UVLO.

9.3.2 Enable (ENx or $\overline{ENx}$)

The logic input of ENx or $\overline{ENx}$ disables all of the internal circuitry while maintaining the power switch OFF. The supply current of the device can be reduced to less than 1 µA when both switches are disabled. A logic low input on $\overline{ENx}$ or a logic high input on ENx enables the driver, control circuits, and power switch of corresponding channel.

The ENx or $\overline{ENx}$ input voltage is compatible with both TTL and CMOS logic levels. The $\overline{FLTx}$ is immediately cleared and the output discharge circuit is enabled when the device is disabled.

9.3.3 Deglitched Fault Reporting

$\overline{FLTx}$ is an open-drain output that asserts (active low) during an overcurrent or overtemperature condition on each corresponding channel. The $\overline{FLTx}$ output remains asserted until the fault condition is removed or the channel is disabled. The TPS20xxC and TPS20xxC-2 dual eliminates false $\overline{FLTx}$ reporting by using internal delay circuitry after entering or leaving an overcurrent condition. The deglitch time is typically 10 ms. This ensures that $\overline{FLTx}$ is not accidentally asserted under overcurrent conditions with a short time, such as starting into a heavy capacitive load. Overtemperature conditions are not deglitched. The $\overline{FLTx}$ pin is high impedance when the device is disabled and in undervoltage lockout (UVLO). The fault circuits are independent so that another channel continues to operate when one channel is in a fault condition.

Feature Description (continued)

9.3.4 Overcurrent Protection

The TPS20xxC and TPS20xxC-2 dual responds to overloads by limiting each channel output current to the static I_{OS} levels shown in *Electrical Characteristics: $T_J = T_A = 25°C$*. When an overload condition is present, the device maintains a constant current (I_{OS}) and reduces the output voltage accordingly, with the output voltage falling to ($I_{OS} \times R_{SHORT}$). Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before voltage is applied to IN. The device senses over-current and immediately switches into a constant-current output. In the second condition, a short or an overload occurs while the device is enabled. At the instant a short-circuit occurs, high currents may flow for several microseconds (t_{IOS}) before the current-limit circuit reacts. The device operates in constant-current mode after the current-limit circuit has responded. In the third condition, the load is increased gradually beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached. The devices are capable of delivering current up to the current-limit threshold without damage. Once the threshold is reached, the device switches into constant-current mode. For all of the above three conditions, the device may begin thermal cycling if the overcurrent condition persists.

9.3.5 Overtemperature Protection

The TPS20xxC and TPS20xxC-2 dual includes per channel overtemperature protection circuitry, which activates at 135°C (minimum) junction temperature while in current limit. There is an overall thermal shutdown of 155°C (minimum) junction temperature when the TPS20xxC and TPS20xxC-2 dual are not in current limit. The device remains off until the junction temperature cools 20°C and then restarts. Thermal shutdown may occur during an overload due to the relatively large power dissipation [($V_{IN} – V_{OUT}$) × I_{OS}] driving the junction temperature up. The power switch cycles on and off until the fault is removed. This topology allows one channel to continue normal operation even if the other channel is in an overtemperature condition.

9.3.6 Softstart, Reverse Blocking and Discharge Output

The power MOSFET driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality.

The TPS20xxC and TPS20xxC-2 dual power switch will block current from OUT to IN when turned off by the UVLO or disabled.

The TPS20xxC dual includes an output discharge function on each channel. A 470 Ω (typical) discharge resistor will dissipate stored charge and leakage current on OUTx when the device is in UVLO or disabled. However as this circuit is biased from IN, the output discharge will not be active when IN voltage is close to 0 V.

The TPS20xxC-2 does not have this function. The output is be controlled by an external loadings when the device is in ULVO or disabled.

9.4 Device Functional Modes

There are no other functional modes.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (for example, keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts or self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS20xxC and TPS20xxC-2 can provide power distribution solutions to many of these device classes.

10.2 Typical Application

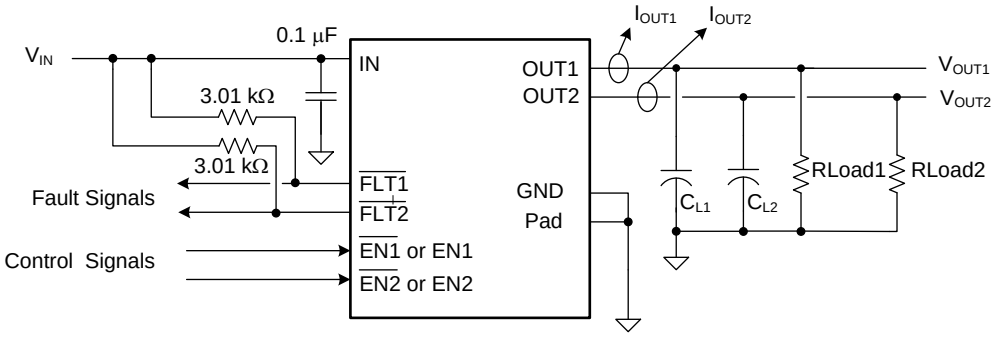


Figure 31. Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

Table 3 shows the design requirements for the typical application.

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage	5 V
Output voltage 1	5 V
Output voltage 2	5 V
Current limit	1 A

10.2.2 Detailed Design Procedure

10.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device. For all applications, TI recommends placing a 0.1-µF or greater ceramic bypass capacitor between IN and GND as close as possible to the device for local noise de-coupling. The actual capacitance should be optimized for the particular application. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce the overshoot voltage from exceeding the absolute maximum voltage of the device during heavy transients.

A 120-µF minimum output capacitance is required when implementing USB standard applications. Typically this uses a 150-µF electrolytic capacitor. If the application does not require 120 µF of output capacitance, a minimum of 10-µF ceramic capacitor on the output is recommended to reduce the transient negative voltage on OUTx pin caused by load inductance during a short circuit. The transient negative voltage should be less than 1.5 V for 10 µs.

10.2.3 Application Curves

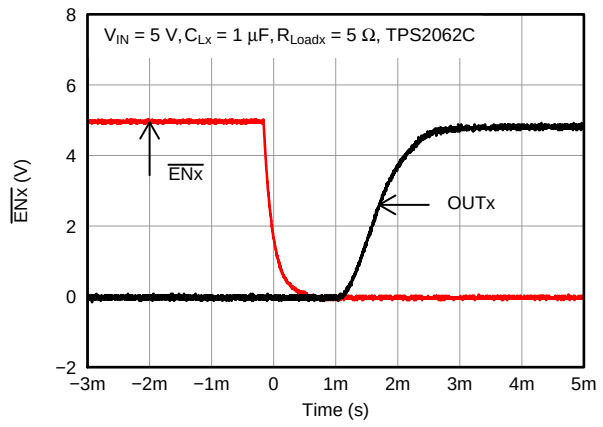


Figure 32. TPS2062C Turnon Delay and Rise Time With 1-µF Load

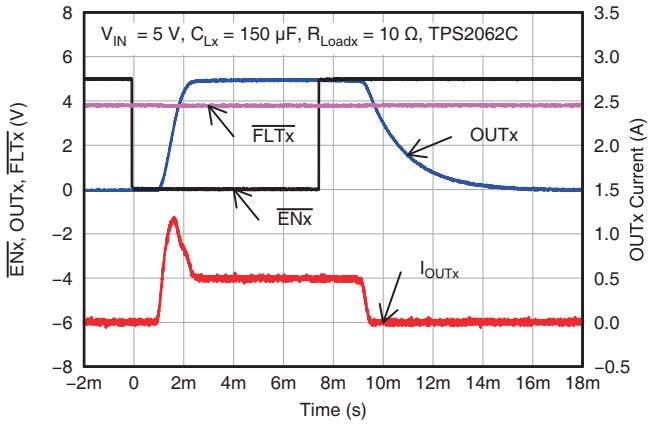


Figure 33. TPS2062C Enable/Disable into 10-Ω Load

11 Power Supply Recommendations

11.1 Self-Powered and Bus-Powered Hubs

A Self-Powered Hub (SPH) has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller.

Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A Bus-Powered Hub (BPH) obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and it is limited to 500 mA from an upstream port.

11.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-powered functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

12 Layout

12.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace.
- When large transient currents are expected on the output, TI recommends placing a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin.
- The PowerPAD should be directly connected to PCB ground plane using wide and short copper trace.

12.2 Layout Example

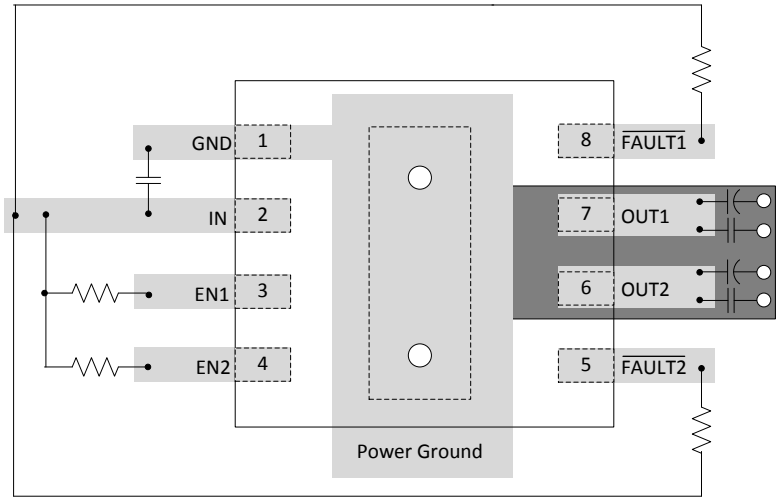


Figure 34. Layout Recommendation

12.3 Power Dissipation and Junction Temperature

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS20xxC and TPS20xxC-2 dual. The system designer can control choices of package, proximity to other power dissipating devices, and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors such as airflow and maximum ambient temperature are often determined by system considerations.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical.

The following procedure requires iteration because power loss is due to the two internal MOSFETs $2 \times I^2 \times r_{DS(on)}$, and $r_{DS(on)}$ is a function of the junction temperature. As an initial estimate, use the $r_{DS(on)}$ at 125°C from the typical characteristics, and the preferred package thermal resistance for the preferred board construction from the thermal parameters section.

$$T_J = T_A + [2 \times I_{OUT}^2 \times r_{DS(on)} \times \theta_{JA}] \quad (1)$$

where

- I_{OUT} = rated OUT pin current (A)
- $r_{DS(on)}$ = Power switch on-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, look up a new value of $r_{DS(on)}$ and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction and/or package with lower θ_{JA}.

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2052C	Click here	Click here	Click here	Click here	Click here
TPS2062C	Click here	Click here	Click here	Click here	Click here
TPS2062C-2	Click here	Click here	Click here	Click here	Click here
TPS2066C	Click here	Click here	Click here	Click here	Click here
TPS2066C-2	Click here	Click here	Click here	Click here	Click here
TPS2060C	Click here	Click here	Click here	Click here	Click here
TPS2064C	Click here	Click here	Click here	Click here	Click here
TPS2064C-2	Click here	Click here	Click here	Click here	Click here
TPS2002C	Click here	Click here	Click here	Click here	Click here
TPS2003C	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

PowerPad, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2002CDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VFEQ	Samples
TPS2002CDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VFEQ	Samples
TPS2003CDRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VRFQ	Samples
TPS2003CDRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VRFQ	Samples
TPS2052CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYNI	Samples
TPS2052CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYNI	Samples
TPS2060CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRAQ	Samples
TPS2060CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRAQ	Samples
TPS2062CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062C	Samples
TPS2062CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRBQ	Samples
TPS2062CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRBQ	Samples
TPS2062CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2062C	Samples
TPS2062CDRBR-2	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYVI	Samples
TPS2062CDRBT-2	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PYVI	Samples
TPS2064CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRCQ	Samples
TPS2064CDGN-2	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYTI	Samples
TPS2064CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRCQ	Samples
TPS2064CDGNR-2	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYTI	Samples
TPS2066CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066C	Samples
TPS2066CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VRDQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2066CDGN-2	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYUI	Samples
TPS2066CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VRDQ	Samples
TPS2066CDGNR-2	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PYUI	Samples
TPS2066CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2066C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

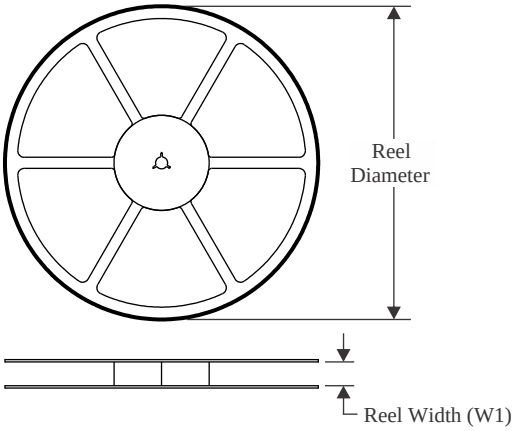
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

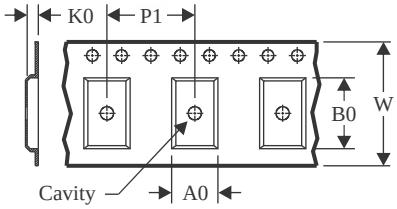
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

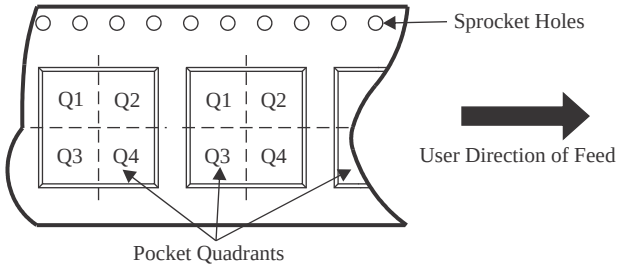


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

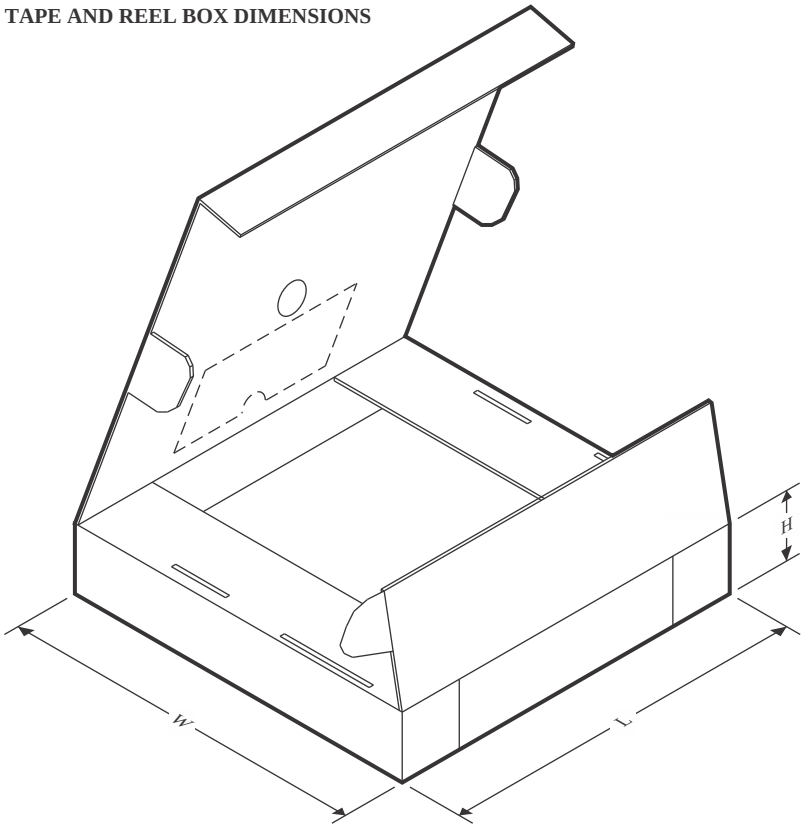
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2002CDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2002CDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2003CDRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2003CDRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2052CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2060CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2062CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2062CDRBR-2	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2062CDRBT-2	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2064CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2064CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066CDGNR-2	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2066CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

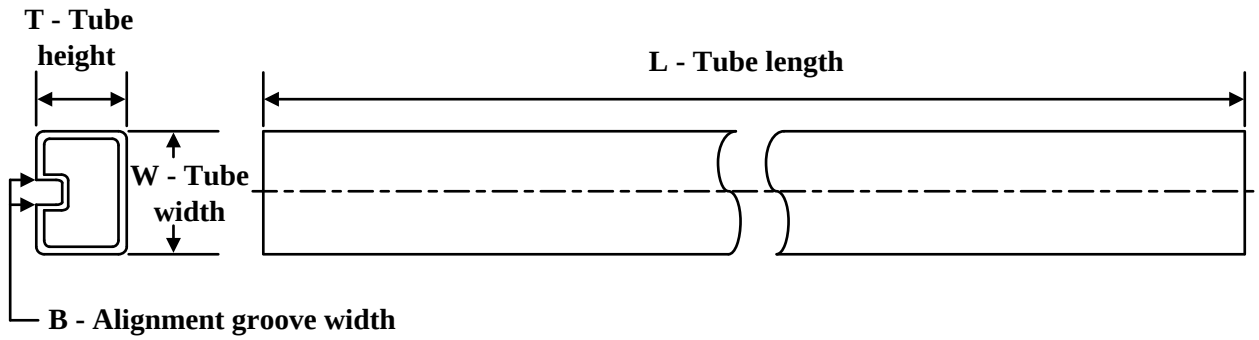
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

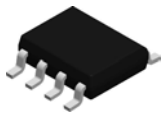
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2002CDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2002CDRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS2003CDRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2003CDRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS2052CDGNR	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2060CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2062CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2062CDR	SOIC	D	8	2500	340.5	336.1	25.0
TPS2062CDR	SOIC	D	8	2500	356.0	356.0	35.0
TPS2062CDRBR-2	SON	DRB	8	3000	367.0	367.0	35.0
TPS2062CDRBT-2	SON	DRB	8	250	182.0	182.0	20.0
TPS2064CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2064CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2066CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
TPS2066CDGNR-2	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS2066CDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2052CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2060CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2062CD	D	SOIC	8	75	507	8	3940	4.32
TPS2062CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2064CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2064CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066CD	D	SOIC	8	75	507	8	3940	4.32
TPS2066CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
TPS2066CDGN-2	DGN	HVSSOP	8	80	330	6.55	500	2.88

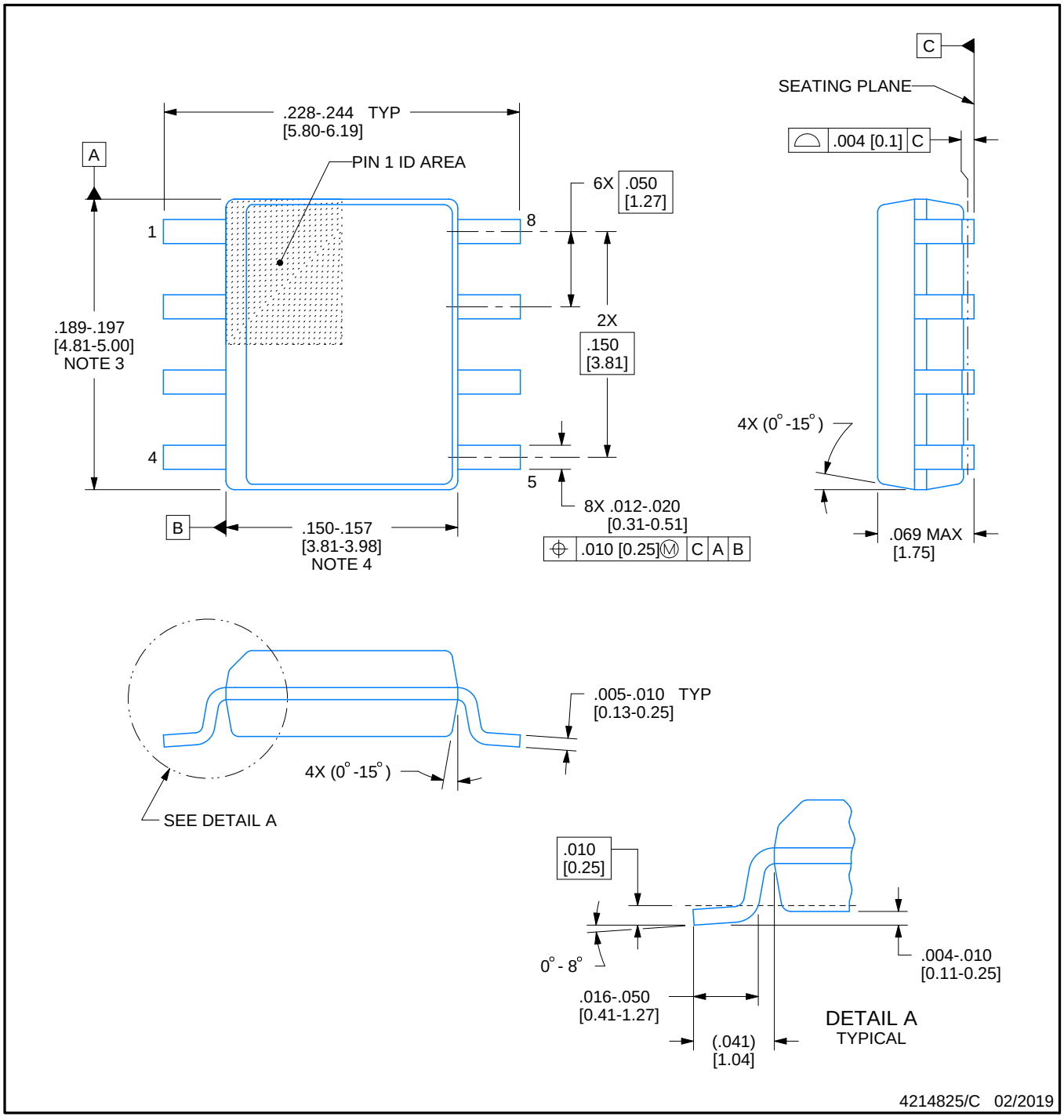


PACKAGE OUTLINE

D0008A

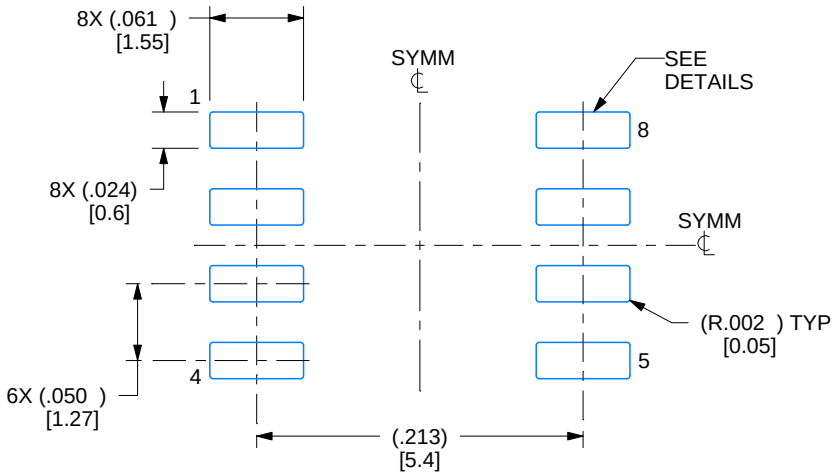
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

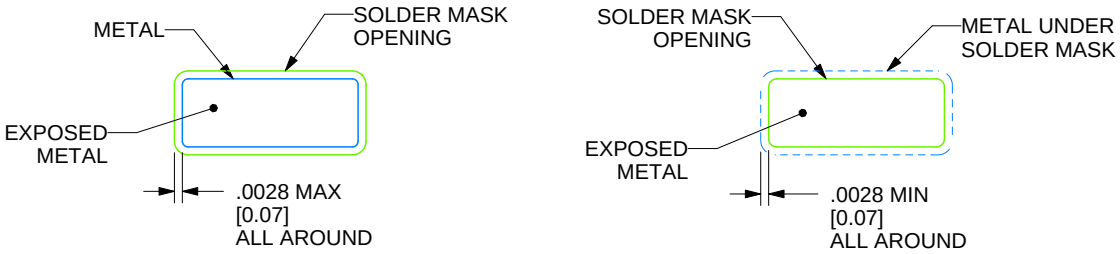


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

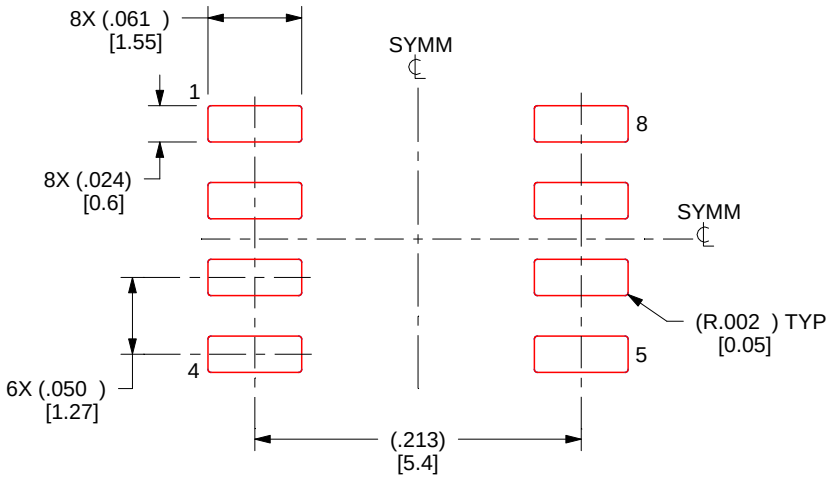
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

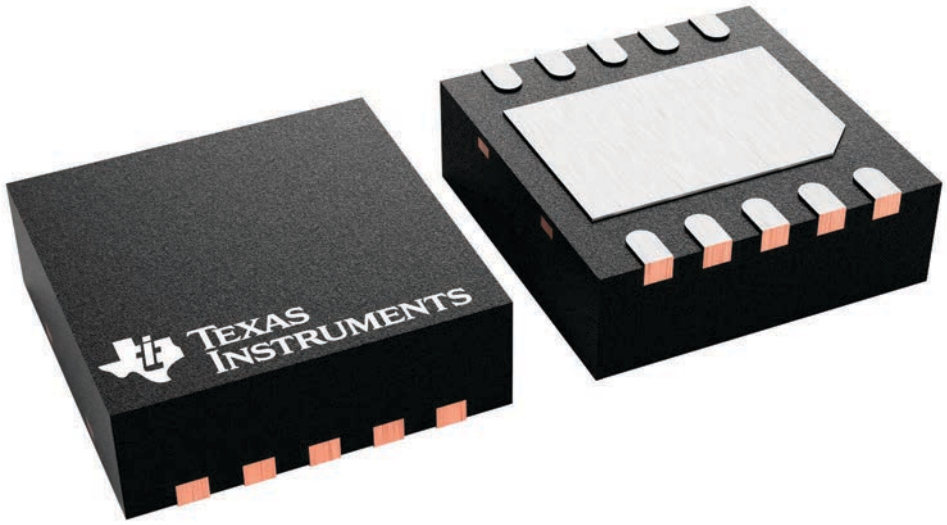
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



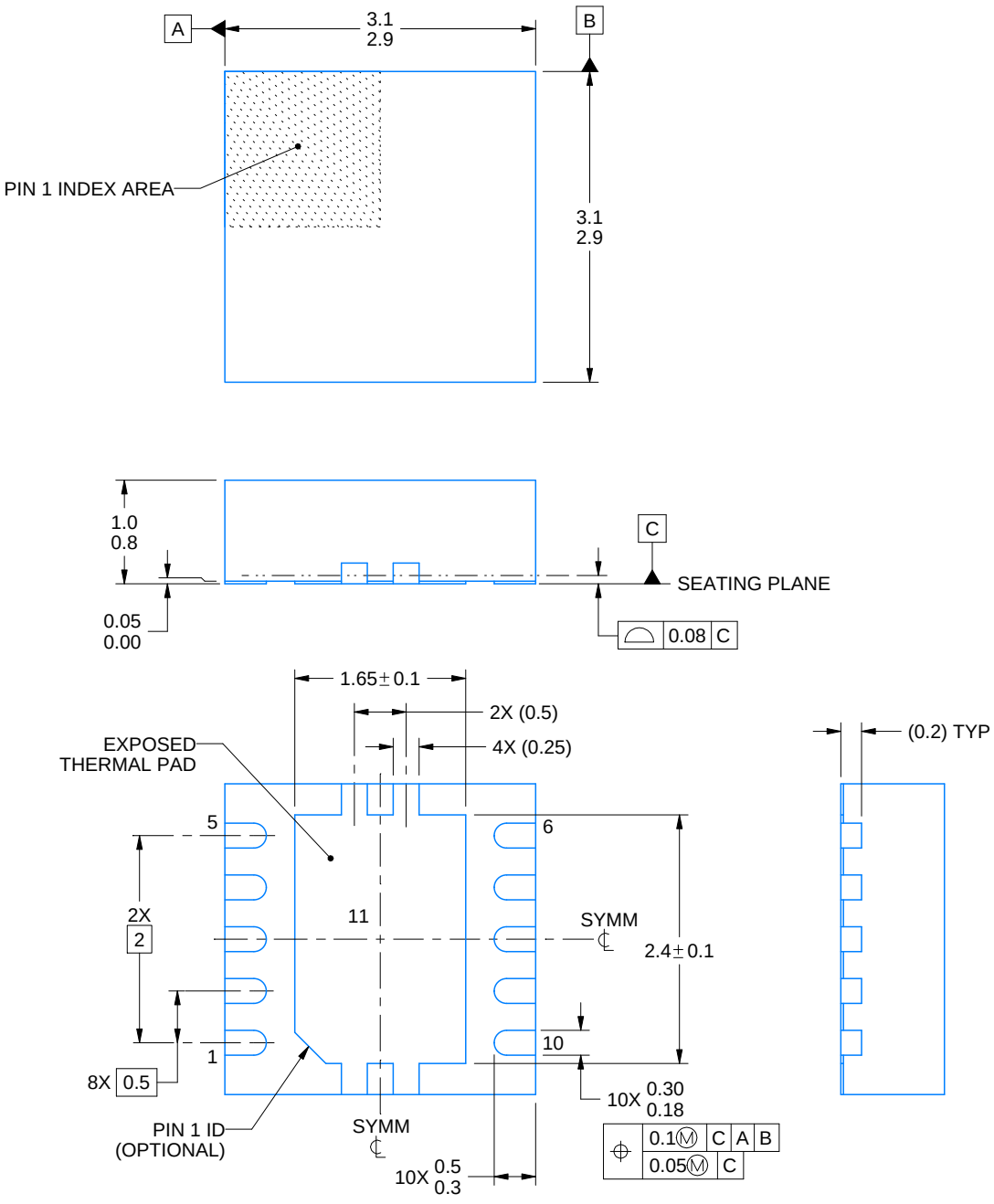
4226193/A

DRC0010J

PACKAGE OUTLINE

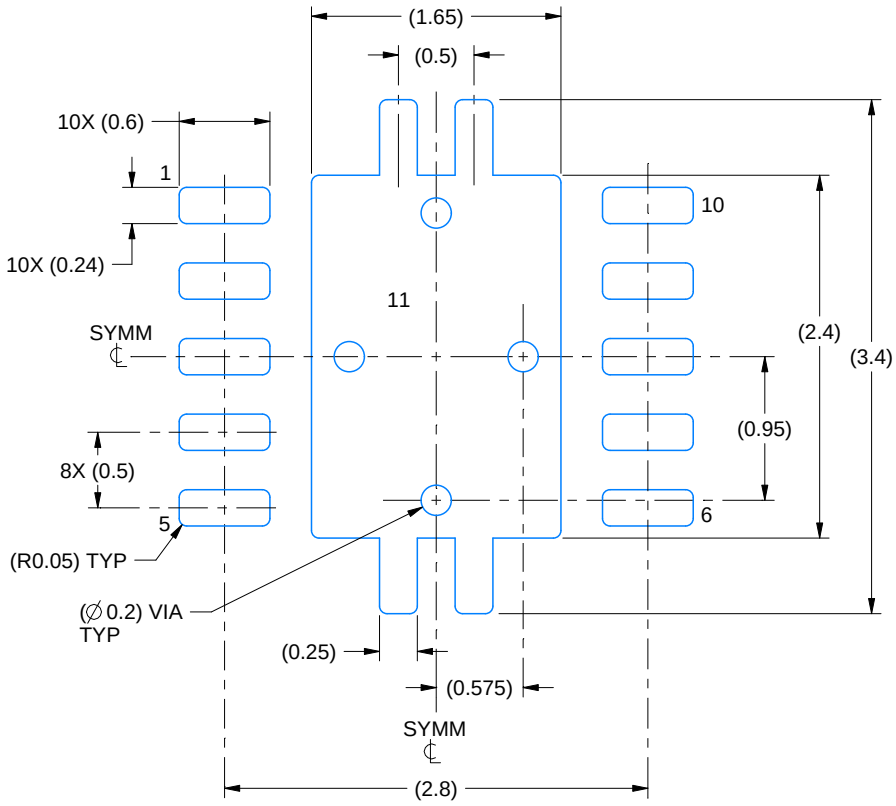
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

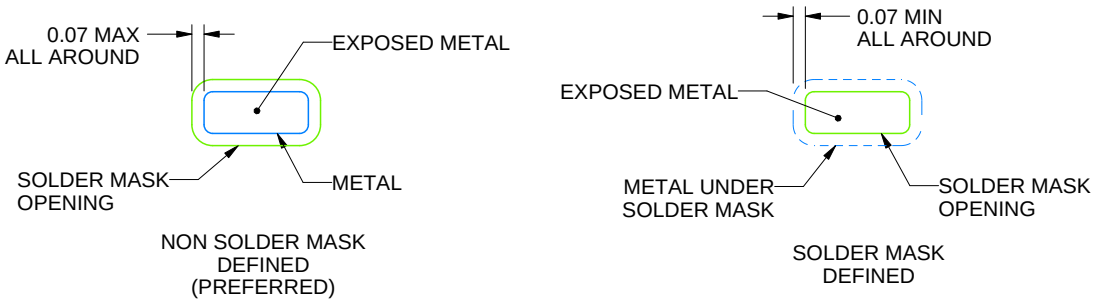


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

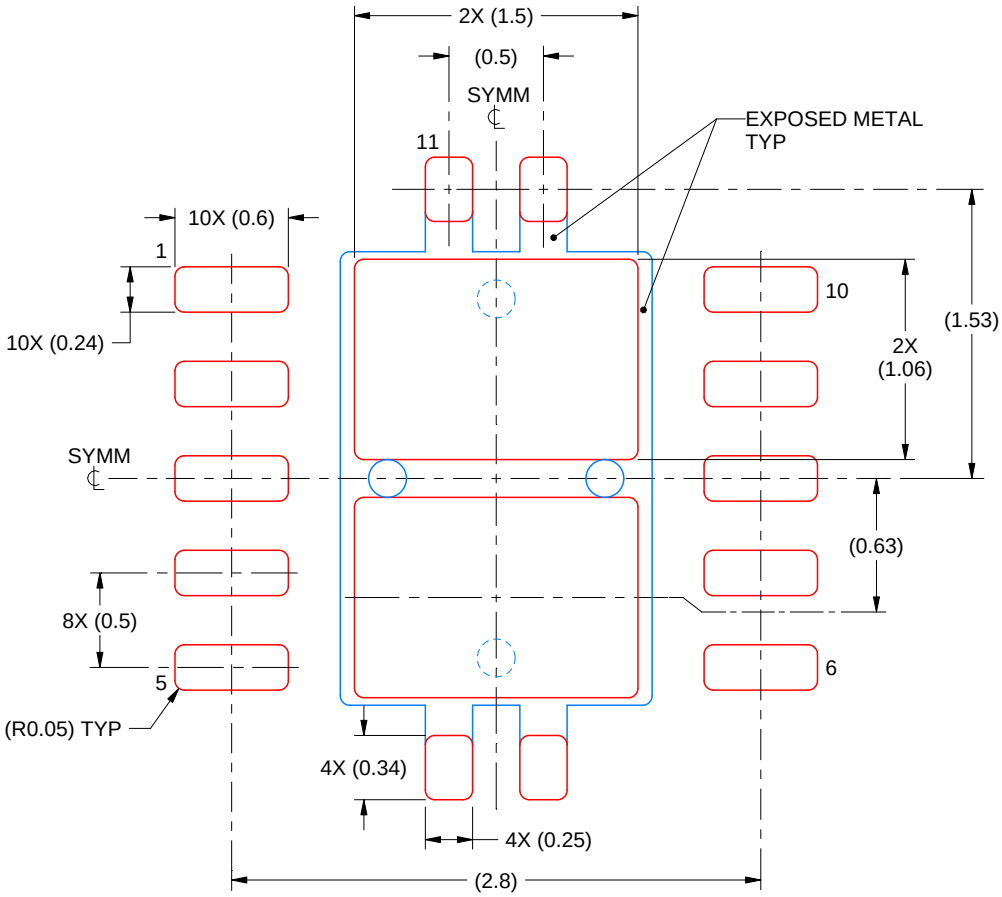
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

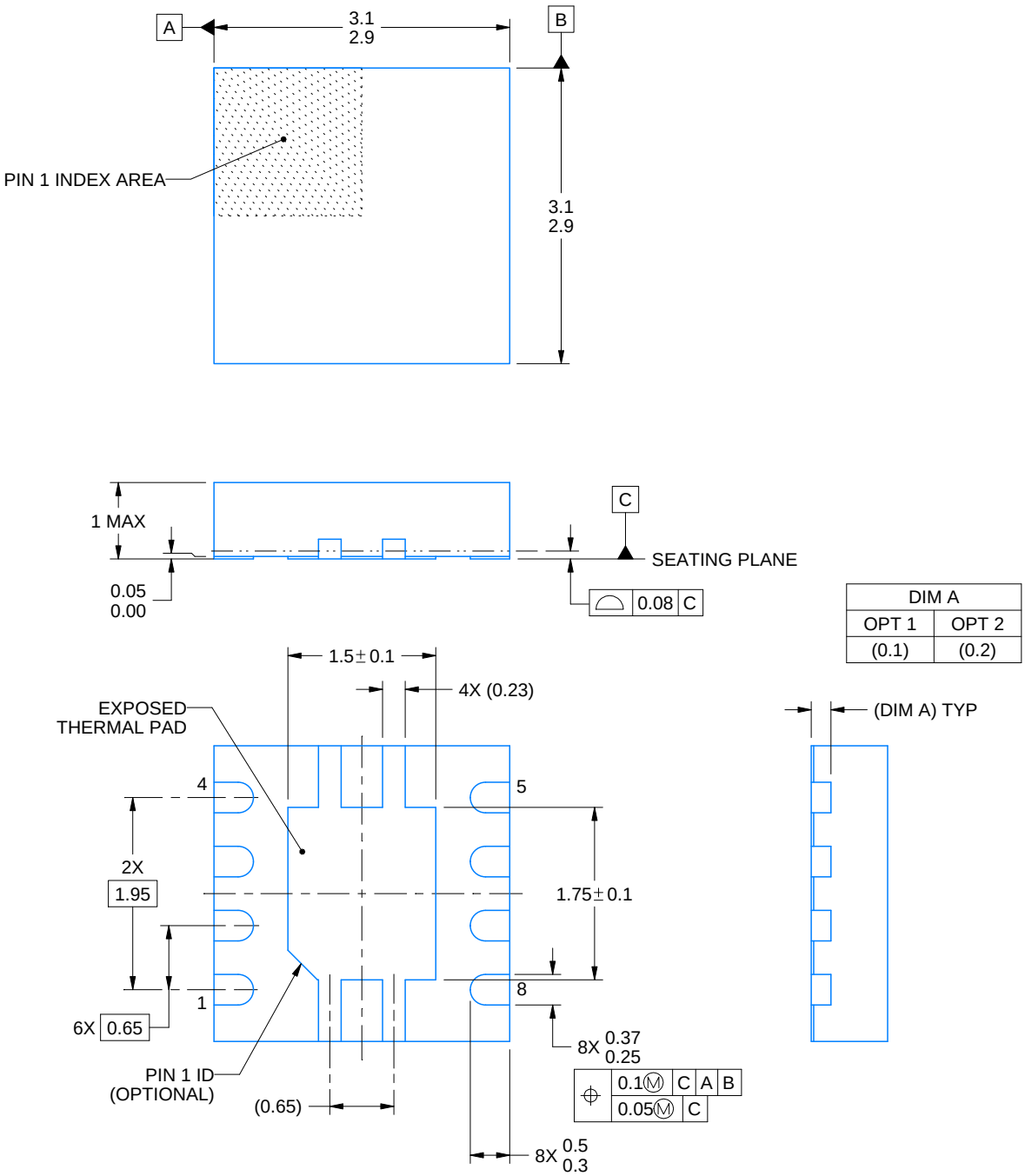
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

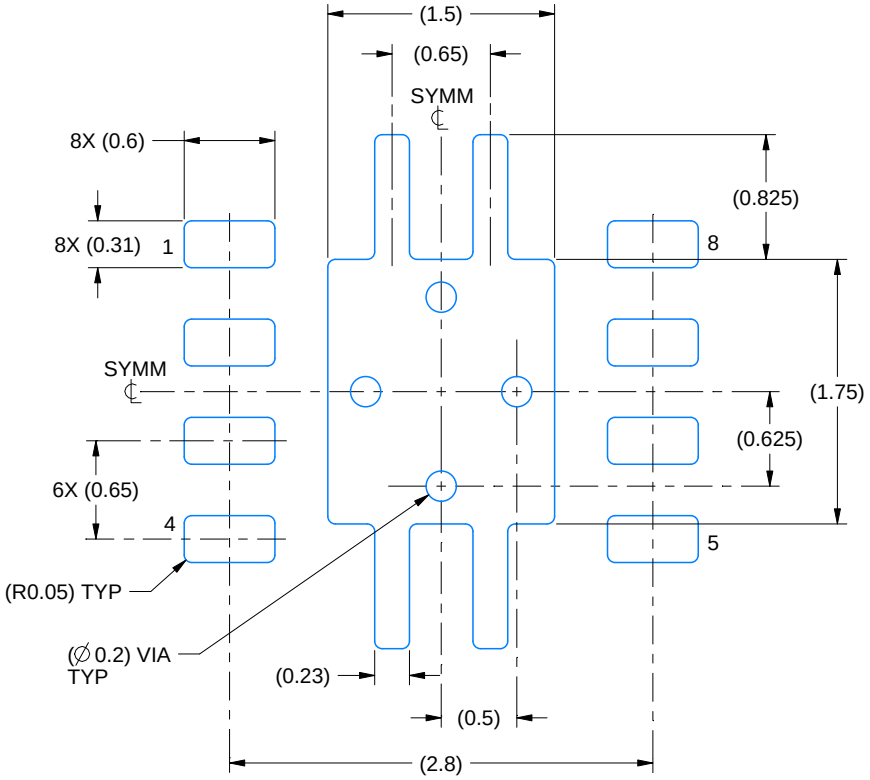
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

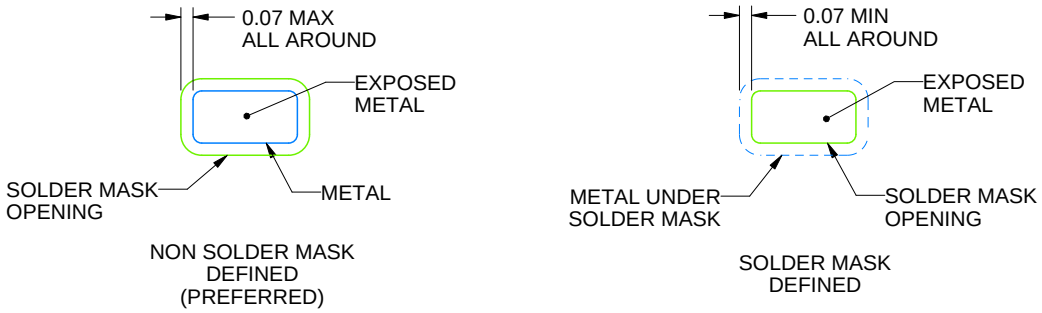
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

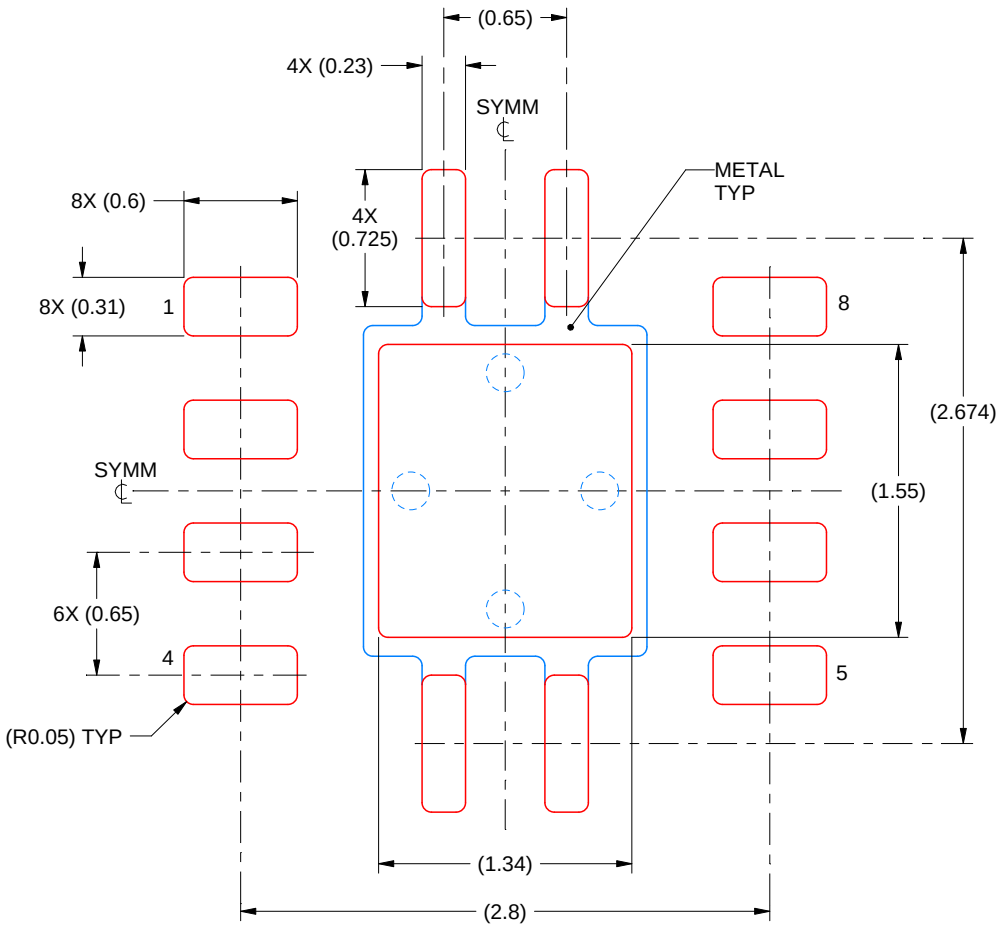


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

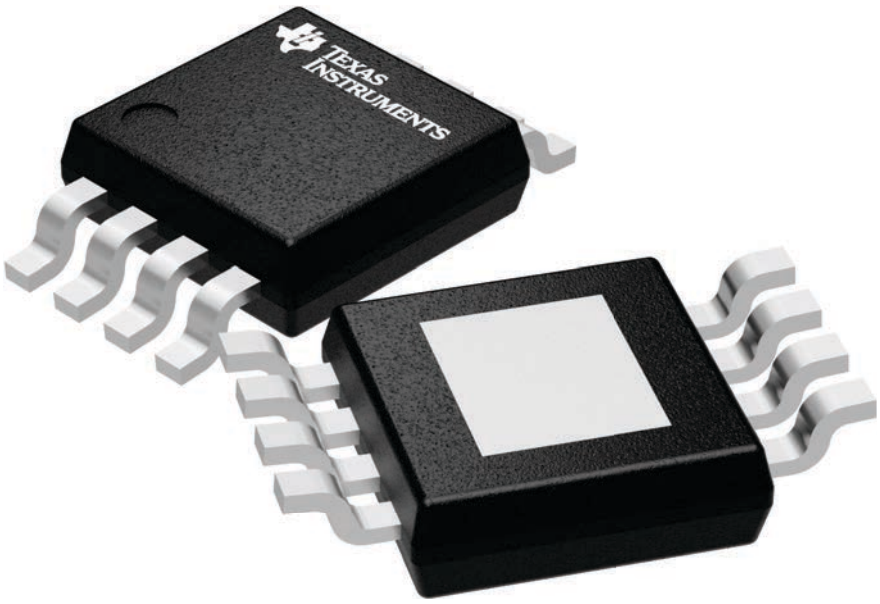
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

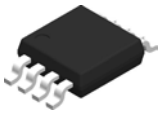
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

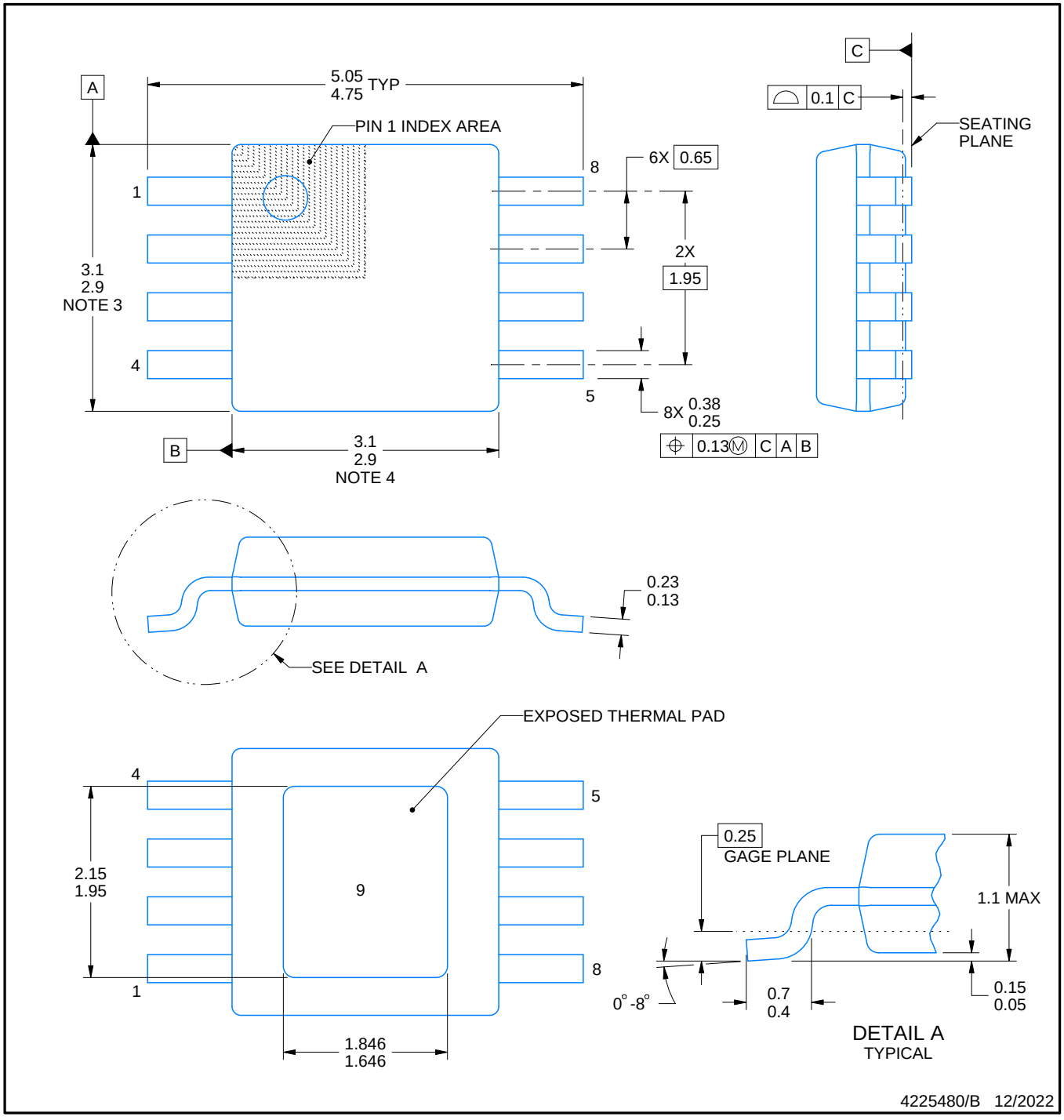
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

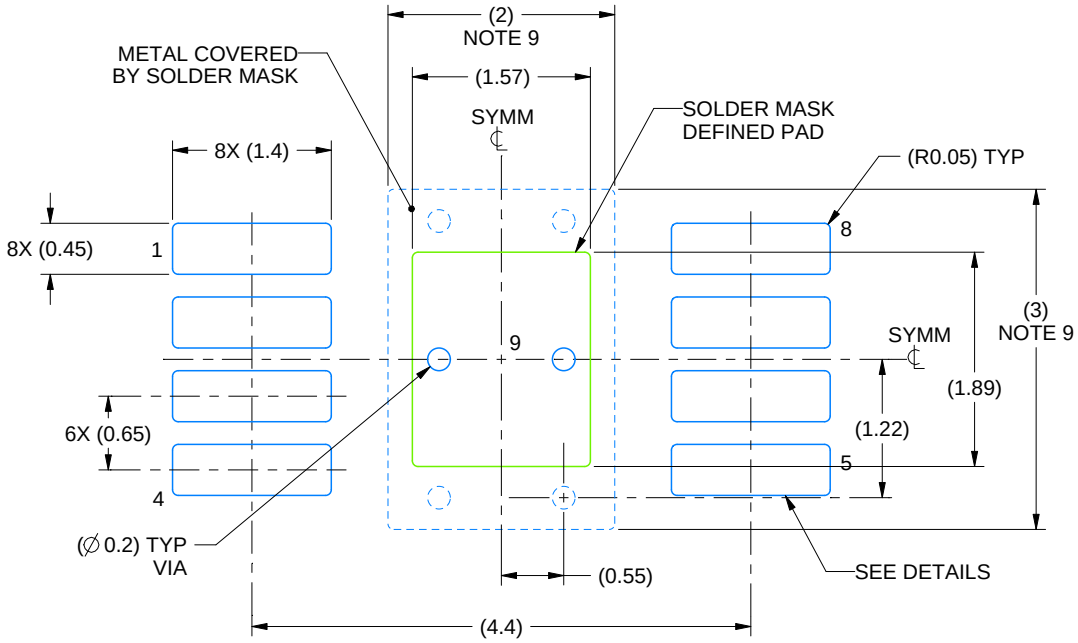
SMALL OUTLINE PACKAGE



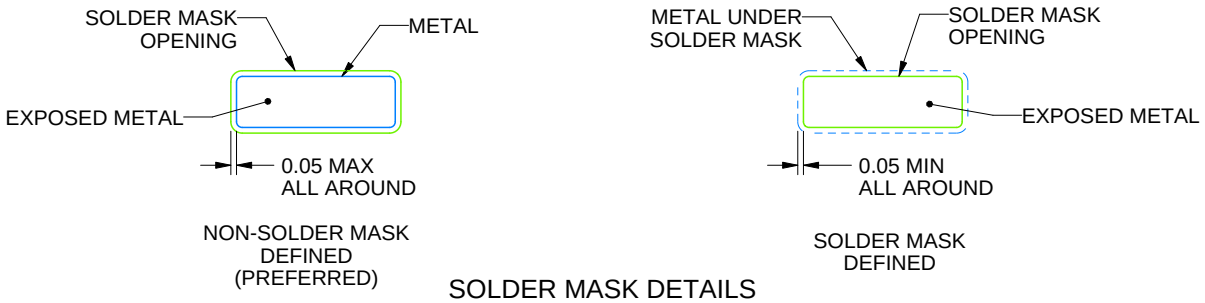
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

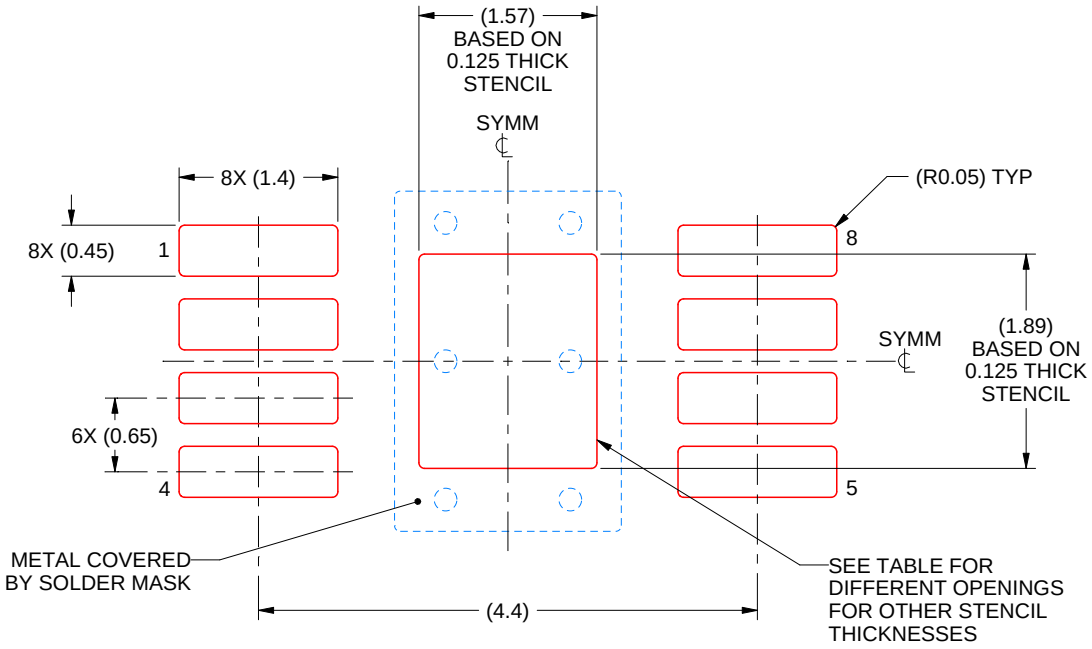


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265