



PCN Number: SM110416 Chgnot.doc rev 13 1/14

Product/Process Change Notification (PCN)

Customer: Digi-Key	Date: 11/04/2016
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Customer Part # and/or Lot# affected: A8450KLBTR-T

Originator: Scott Mitti	Phone: 508-854-5627
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Duration of Change:	Permanent	Tempora	ry (explain)	
Summary description of change: Part Change:	Process	Change: X	Other:	

- 1. Allegro currently manufactures the A8450KLBTR-T on the 6" wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA. Allegro will phasing out the 6" wafer line and will transition manufacturing to the 8" ABCD4 technology wafer fab line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA
- 2. The A8450KLBTR-T will have an additional final test location: Allegro MicroSystems (Thailand) Co., Ltd. (AMTC).

What is the part or process changing from (provide details)?

- 1. Allegro currently manufactures the A8450KLBTR-T on the 6" wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA, The 6" ABCD4 wafer fab line will be phased out.
- 2. In addition to the current Allegro MicroSystems, LLC test facility location in Manila, Philippines, a second test facility referred to as Allegro MicroSystems (Thailand) Co., Ltd. (AMTC) located in Saraburi, Thailand will be added as a primary site.

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

- 1. The A8450KLBTR-T will transition manufacturing to the 8 inch wafer fab ABCD4 technology line at Polar Semiconductor LLC (PSL), Bloomington, MN, USA..
- 2. Allegro will be expanding its manufacturing capabilities with the addition of a new, wholly-owned integrated circuit test facility located in Saraburi, Thailand. The same make and model test equipment will be utilized and test site transfer buy off data will be on file for each device before production begins.





Note: Validation of equivalence within a specific application is at the discretion of the Customer

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Is a PPAP update required?	Yes	No X
Is reliability testing required? (If Yes, refer to attached plan)	Yes X	No (explain)

Reliability Qualification Results

Device: 8450 (8451)
Fab Lot #: 1534215KAAA
Fab Location: PSL
Package: LB (SOIC)

Number of Leads: 24
Assembly Location: Carsem
Tracking Number: 3141, 3643
Lead Finish: 100% Sn

Reason For Qualification: 8450 (8451) - Automotive Multioutput Voltage Regulator

Reliability Qualification Results						
8450 (8451) - STR#3141, 3643			Requirements			
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results
Preconditioning	PC	A1	JESD22-A113 / J-STD-020	30°C/60% RH, 192 hrs, Peak Reflow=260°C; MSL3, (HAST, AC, TC)	231	0 Rejects
HAST	HAST	A2	JESD22-A110	Ta=130°C, 85% RH, 2 ATM, 0, 96 hrs	77	0 Rejects
Autoclave	AC	А3	JESD22-A102	Ta=121°C, 100% RH, 15 PSIG, 0, 96 hrs		0 Rejects
Temperature Cycle	тс	A4	JESD22-A104	Ta = -65°C to +175°C, 0, 500, 1000 Cycles	77	0 Rejects
High Temperature Storage Life	HTSL	A6	JESD22-A103	150°C, 0, 1000 hrs	77	0 Rejects
Wire Bond Pull	WBP	C2	Mil-Std-883 Method 2011	Temp conditions and sample size are of in the test method. (after TC)	defined	0 Rejects; Cpk>1.67
Solderability	SD	C3	JESD22-B102	Meniscograph	22	0 rejects; > 95% Lead Coverage
Heat Resistance to Solder	SD	СЗА	JESD22-B106	85°C/85%RH for 48 hrs; 22 devices	Perform Dip & Loc Cracks or oth abnomalities, confo individual spe	
High Temperature Operating Life	HTOL	B1	JESD22-A108	Ta=125°C, 0, 1000 hrs	77	0 Rejects
Early Life Failure Rate	ELFR	B2	AEC-Q100-008 / JESD22-A108	Ta=125°C, 0, 48 hrs	800	0 Rejects
Electrostatic Discharge Human Body Model	нвм	E2	AEC-Q100-002 / JS-001-2014			Classification H2, HBM = 2.5kV
Electrostatic Discharge Charged Device Model	CDM	E3	AEC-Q100-011			Classification = C6, > 1kV
Latch-Up	LU	E4	JESD78	Test Conditions, Sampling Size are defined in the Test Method Class II, Lev		Class II, Level A
Electrical Distributions	ED	E5	AEC Q100-009			0 Rejects; Cpk>1.67

This device qualification is considered to be passing all environmental stress evaluations per the Allegro MicroSystems, Inc. 900019 and AEC-Q100 specification.

Approved by:

Bob Demers

Product Safety and Reliability Allegro MicroSystems, LLC





Expected completion date for internal qualification: Complete Expected PPAP availability date: N/A Target implementation date: May 2017 Estimated date of first shipment: June 2017 Expected sample availability date: Available Upon Request Yes Date Required: No X Notification Only

Please note: It is our intention to inform our customer of changes as early as possible. Under Allegro's procedure for product/process change notification, Allegro strives, based on its technical judgment, to provide notification of significant changes that may affect form, fit or function. However, as Allegro cannot ensure evaluation of product/process changes for each and every application; the customer retains responsibility to validate the impact of a change on its application suitability. If samples are needed for validation of a change, requests may be made via the contact information provided herein. Please contact your Account Manager or local Sales contact for any questions. We would kindly request your consideration so we can meet our target date for implementation. Unless both parties agree to extend the implementation date, this change will be implemented as scheduled.

Approved by: Date: Title: cc: Allegro Sales/Marketing/Quality

Customer comments/Conditions of Acceptance: