



SANYO Semiconductors

## DATA SHEET

An ON Semiconductor Company

# LV5809MX — Bi-CMOS IC Step-down Switching Regulator

## Overview

LV5809MX is a 1ch step-down switching regulator. 0.2Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current. Low-heat resistance and compact-package MFP8 (200mil) employed. Current mode control type, with superior load current response and easy phase compensation ON/OFF pin, allowing the standby mode with the current drain of 40μA or less Pulse-by-pulse over-current protection and overheat protection available for protection of load devices Soft start pin to be provided with a capacitance for soft start.

## Functions

- 2.5A 1ch step-down switching regulator
- Wide input dynamic range (4.5 to 18V)
- High efficiency (90%  $I_{OUT} = 1A$ ,  $V_{IN} = 12V$ ,  $V_O = 5V$ )
- Standby mode
- Over-current protection
- Thermal shutdown
- Reference voltage: 0.8V
- Fixed frequency: 330kHz
- Soft start
- Compact package: MFP8 (200mil) with Exposed Pad

## Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input $V_{IN}$ voltage	$V_{IN\ max}$		20	V
BOOT pin maximum voltage	$V_{BT\ max}$		25	V
SW pin maximum voltage	$V_{SW\ max}$		$V_{IN\ max}$	V
BOOT pin-SW pin maximum voltage	$V_{BS-SW\ max}$		7	V
EN pin maximum voltage	$V_{EN\ max}$		20	V
FB, COMP, SS pin maximum voltage	$V_{fs\ max}$		7	V
Allowable power dissipation	$P_d\ max$	Mount on a specified board *	2.05	W
Junction temperature	$T_j\ max$		150	°C
Operating temperature	$T_{opr}$		-20 to 80	°C
Storage temperature	$T_{stg}$		-40 to 150	°C

\* Specified board: 46.4mm × 31.8mm × 1.7mm, glass epoxy both side.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

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## Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V <sub>IN</sub> pin voltage	V <sub>IN</sub>		4.5 to 18	V
BOOT pin voltage	V <sub>BT</sub>		-0.3 to 23	V
SW pin voltage	V <sub>SW</sub>		-0.4 to V <sub>IN</sub>	V
BOOT pin-SW pin maximum voltage	V <sub>BS-SW</sub>		6.5	V
EN pin maximum voltage	V <sub>EN</sub>		18	V
FB, COMP, SS pin voltage	V <sub>FSSO</sub>		6	V

## Electrical Characteristics at Ta = 25°C, V<sub>IN</sub> = 12V, unless otherwise specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	I <sub>CC1</sub>	EN=0V		40		μA
IC current drain in operation	I <sub>CC2</sub>	EN=open		2		mA
Efficiency	Effcy	V <sub>IN</sub> =12V, I <sub>O</sub> UT=1A, V <sub>o</sub> =5V, Design target *1		90		%
Reference voltage	V <sub>ref</sub>	V <sub>IN</sub> =4.5V to 18V (±2%)	-2%	0.8	+2%	V
FB pin bias current	I <sub>ref</sub>	FB=0.8V application		10	100	nA
High-side ON resistance	R <sub>onH</sub>	BOOT=5V		0.2		Ω
Oscillation frequency	f <sub>OSC</sub>		265	330	395	kHz
Oscillation frequency during short-circuit protection	f <sub>OSCS</sub>		26	33	40	kHz
EN high-threshold voltage	V <sub>enh</sub>				2.1	V
EN low-threshold voltage	V <sub>enl</sub>		0.8			V
Maximum ON DUTY	D max			80		%
Current limit peak value 1	I <sub>c1</sub>	V <sub>IN</sub> =12V, V <sub>O</sub> UT=5V, L=10μH	2.7		5.3	A
Current limit peak value 2	I <sub>c2</sub>	V <sub>IN</sub> =12V, V <sub>O</sub> UT=3.3V, L=10μH	3.0		5.6	A
Current limit peak value 3	I <sub>c3</sub>	V <sub>IN</sub> =12V, V <sub>O</sub> UT=1.2V, L=10μH	3.3		5.9	A
Thermal shutdown temperature	T <sub>tsd</sub>	*Design guarantee *2		160		°C
Thermal shutdown temperature hysteresis	D <sub>tsd</sub>	*Design guarantee *2		40		°C
Soft start current	I <sub>SS</sub>	SS=0V	6	10	14	μA

\*1: Reference value (not tested before shipment)

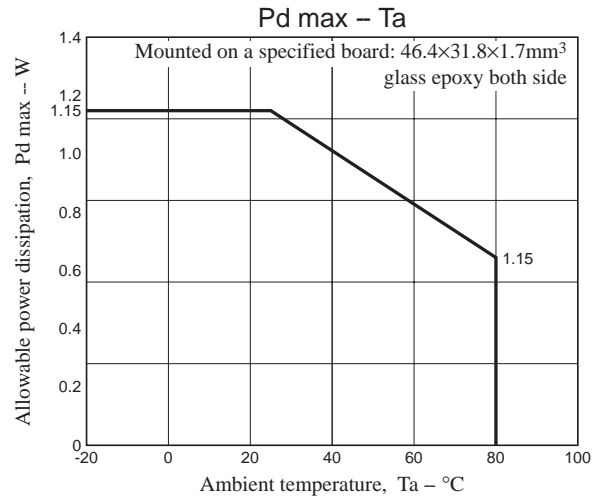
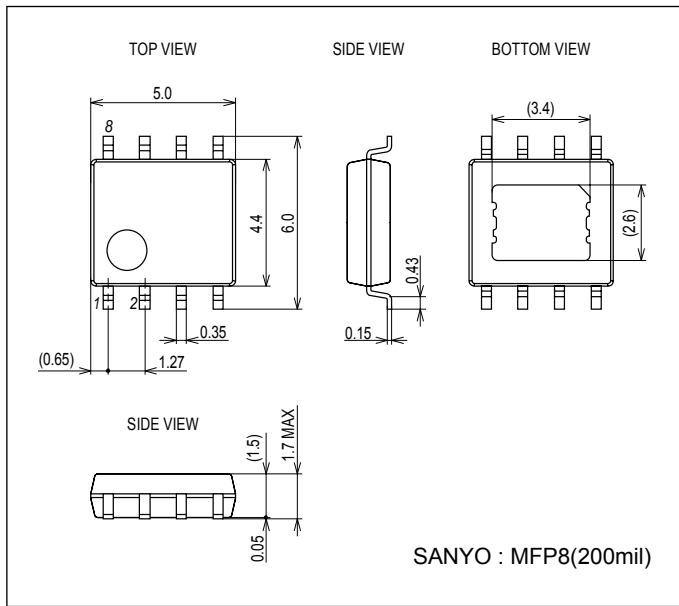
\*2: Design guarantee (value guaranteed by design and not tested before shipment)

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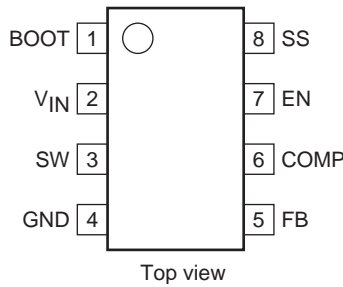
## Package Dimensions

unit : mm (typ)

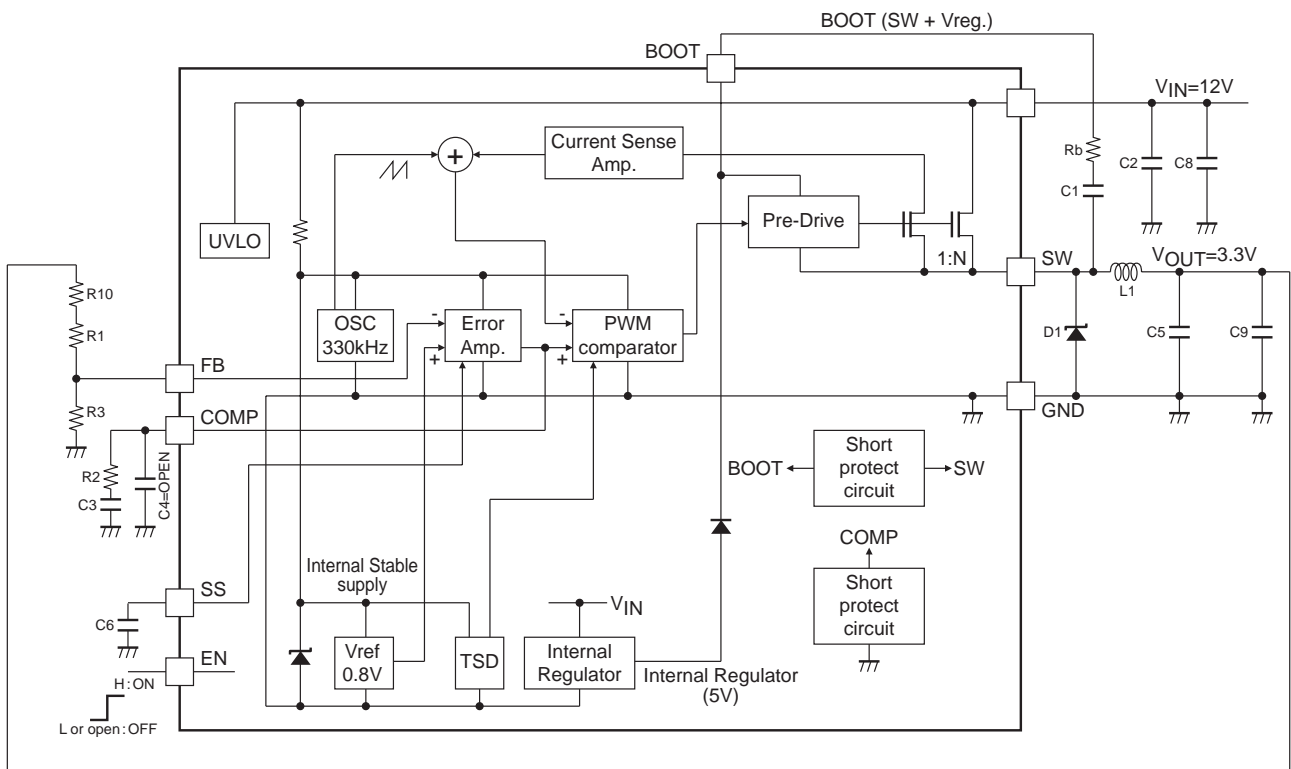
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## Pin Assignment



## Block Diagram and Sample Application Circuit (3.3V output)



• C1,C8,C5,C9 = ceramic capacitor used.

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## Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.022μF between SW pins.  To protect the SW pin's absolute maximum rating, to ensure stable operation, and to eliminate noise, the boot capacitance serial resistance (about 100Ω) Rb proves effective.	
2	V <sub>IN</sub>	Input voltage pin. Connect substantially large (10μF 2 parallel or more) capacitance between this pin and GND.	
3	SW	Power switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	
4	GND	Ground pin.	
5	FB	Feedback pin. Sets the output voltage by means of split resistor in the section of the output voltage V <sub>OUT</sub> - FB - GND. V <sub>OUT</sub> setting is made as calculated below:  $V_{OUT} = V_{ref} \times \left\{ 1 + \frac{(R1 + R10)}{R3} \right\}$ $V_{ref} = 0.8V$ Example: 3.3V output voltage (See Block Diagram and Sample Application Circuit)  $V_{OUT} = V_{ref} \times \left\{ 1 + \frac{(27k + 4.3k)}{10k} \right\}$ $= 3.304V$	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 10μA source voltage and external soft start capacity. The soft start capacity C6 can be set as follows:  $C6 = 10\mu A \times \frac{T_{ss}}{V_{ref}}$ Where, T <sub>ss</sub> is the soft start time and V <sub>ref</sub> is the reference voltage. Example: 1.2ms soft start time achieved  $C6 = 10\mu A \times \frac{1.2ms}{0.8V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.	

## Considerations for the design

- During use with  $V_{IN} = 12V$  or less, the boot strap voltage may become deficient due to intermittent operation at no load, resulting in failure of normal operation. In this case, insert a resistance of about  $500\Omega$  between  $V_{OUT}$  and GND and avoid the intermittent operation mode during use.
- Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance  $R_b$ .

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