PCN Number	20210202001 <mark>B</mark> .2					PCN	Date:	June 23, 2021		
Title:	Qualify UMC-F	12A for C0	21.4	Process	as alternate source	ce				
<b>Customer C</b>	Contact:	PCN Mana	iger				Dept	: Q	uality Services	
Proposed 1	st Ship Date:	August 9,	202	21	Estimated Sa Availabilit	-	ole		provided at ole request	
Change Type	pe:									
Assemb	ly Site	Design				Wafer Bump Site				
Assemb	ly Process			Data Sheet			Wa	fer Bu	mp Material	
Assemb	ly Materials			Part nu	Part number change			Wafer Bump Process		
Mechan	ical Specificatio	n		Test Sit	Test Site			fer Fal	Site	
Packing	/Shipping/Labe		Test Pro	Test Process		Wa	fer Fal	Materials		
							Wa	fer Fal	Process	
	PCN Details									

# Description of Change:

Texas Instruments Incorporated is announcing the qualification of Wafer Fab site UMC-F12A in the C021.A process as an alternate source.

# The purpose of Addendum B is to include additional part numbers as highlighted under Product Affected section on page 4.

Proposed 1<sup>st</sup> Ship Date for the new devices will be 180 days from this notice (Dec. 23, 2021). The Proposed 1<sup>st</sup> Ship Date of Aug 9, 2021 still applies for the original set of devices.

	Current Fab Site		Alternate Fab Site				
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter		
DMOS6	C021.A	300 mm	UMC-F12A	C021.A	300 mm		

# **Process Difference Summary**

Description	Current Fab	New Fab
Wafer Fab Site	DM6	UMC12A
Dielectric Material	SiCN/TEOS/LK SiOC (Stack effective k value = 3.1)	SiCN/LK SiOC (Stack effective k value = 3.1)
Top protective layer or Passivation layer material	PO Oxide (TEOS/SiON)	TEOS/SiN

### **Reason for Change:**

Continuity of Supply.

#### Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

None.

# **Changes to product identification resulting from this PCN:**

#### **Current:**

Current Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
DMOS6	DM6	USA	Dallas
New Fab Site:			
Now Chin Cita	Chin Cita Origin Coda (201)	Chin Cita Country Codo (211)	Chin Cita City

New Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
UMC-F12A	F12	TWN	Tainan

# Sample Product Shipping Label (not actual product label)

TEXAS INSTRUMENTS MADE IN: Malaysia 2DC: 2Q:

MSL 2 /260C/1 YEAR SEAL DT

(1P) SN74LS07NSR (D) 0336 31T)LOT: 3959047MLA 4W) TKY(1T) 7523483SI2

(2P) REV: (20L) CSO: SHE (22L) ASO: MLA

(V) 0033317 (21L) CCO:USA (23L) ACO: MYS

OPT: ITEM: (L)T0:1750 LBL:

MSL 1 /235C/UNLIM 03/29/04

#### **Product Affected:**

DS90UB936TRGZRQ1

DS90UB936TRGZTQ1

DS90UB954TRGZRQ1

DS90UB954TRGZTQ1

DS90UB958TRGZRQ1

DS90UB958TRGZTQ1

DS90UB960WRTDRQ1

DS90UB960WRTDTQ1

DS90UB962WRTDRQ1

DS90UB962WRTDTQ1

DS90UB934TRGZRQ1 <- See Qualification report on page 8.

DS90UB934TRGZTQ1 <- See Qualification report on page 8.

**Automotive New Product Qualification Summary** 

(As per AEC-Q100 and JEDEC Guidelines)

## Approved 27-Jan-2021 **Product Attributes**

Attributes	Qual Device: DS90UB960WRTD	Qual Device: DS90UB954TRGZTQ 1	QBS Process Reference: DS90UB964TRGCRQ1	QBS Reference: DS90UB960WRTDRQ1	QBS Reference: DS90UH949TRGCRQ1
Automotive Grade Level	Grade 2	Grade 2	Grade 2	Grade 2	Grade 2
Operating Temp Range	-40 to +105 C	-40 to +105 C	-40 to +105 C	-40 to +105 C	-40 to +105 C
<b>Product Function</b>	Signal Chain	-	Interface	Signal Chain	Signal Chain
		Die	e Attributes		
Wafer Fab Supplier	UMC-12A	UMC-12A	UMC-12A	DMOS6	DMOS6
Wafer Diameter (mm)	300	300	300	300	300
Wafer Process ID	1118C021.A6	1118C021.A6	1118C021.A6	1118C021.A6	1118C021.A6
Wafer Process Technology	C021	C021	C021.	C021	C021
		Pack	age Attributes		
Assembly Site	AP1	CLARK-AT	CLARK AT	AP1	CLARK AT
Package Type	VQFN	VQFN	VQFN	VQFN	VQFN
Package Designator	RTD	RGZ	RGC	RTD	RGC
Ball/Lead Count	64	48	64	64	64
Package Size (mils)	354.33 X 354.33	275.59 X 275.59	354.33 X 354.33	354.33 X 354.33	354.33 X 354.33
Body Thickness (mils)	39.37	35.43	39.37	39.37	39.37

QBS: Qual By Similarity
 Qual Devices qualified at LEVEL3-260C: DS90UB960WRTD
 Qual Devices qualified at LEVEL3-260C: DS90UB954TRGZ

#### **Qualification Results**

						Data [	Displayed	as: Number of lots	/ Total sample siz	e / Total failed		
Туј	pe	#	Test Spec	Mi n Lo t Qt y	SS / Lo t	Test Name / Condition	Duratio n Test (	Qual Device: DS90UB960WRTD RQ1 Group A – Accelerated	Qual Device: DS90UB954TRGZ TQ1 Environment Stress T	QBS Process Reference: DS90UB964TRGC RQ1	QBS Reference: DS90UB960WRTD RQ1	QBS Reference: DS90UH949TRGC RQ1
			JEDEC					-p				
P	С	A 1	J-STD- 020 JESD2 2-A113	3	77	Automotive Preconditioni ng	Level 3- 260C	-	-	3/Pass	2/Pass	1/Pass
HA	ST	A 2	JEDEC JESD2 2-A110	3	77	Biased HAST, 110C/85%RH	528 Hours	-	-	3/231/0	-	-
HA	ST	A 2	JEDEC JESD2 2-A110	3	77	Biased HAST, 130C/85%RH	96 Hours	-	-	-	2/154/0	1/77/0
HA	ST	A 2	JEDEC JESD2 2-A110	3	77	Biased HAST, 130C/85%RH	192 Hours	-	-	-	2/154/0	1/77/0
A	С	A 3	JEDEC JESD2 2-A102	3	77	Autoclave 121C	96 Hours	-	-	-	2/154/0	1/77/0
A	С	A 3	JEDEC JESD2 2-A102 JEDEC	3	77	Autoclave 121C Unbiased	192 Hours	-	-	-	2/154/0	1/77/0
UH. T		A 3	JESD2 2-A118 JEDEC	3	77	HAST, 110C/85%RH	264 Hours	-	-	3/231/0		-
Т	С	A 4	JESD2 2-A104 and Append ix 3	3	77	Temperature Cycle, - 65/150C	500 Cycles	-	-	3/231/0	2/154/0	1/77/0
Т	С	A 4	JEDEC JESD2 2-A104 and Append ix 3	3	77	Temperature Cycle, - 65/150C	1000 Cycles	-	-	3/219/0	2/154/0	1/77/0
TC Bi		A 4	JEDEC JESD2 2-A104 and Append ix 3	3	77	Post Temp. <u>Gyele</u> , Bond Pull	Wires	-	-	1/30/0	1/3/0	-
PT	гс	A 5	JEDEC JESD2 2-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	N/A	NA	NA	NA
HT	SL	A 6	JEDEC JESD2 2-A103	1	45	High Temp Storage Bake 150C	1000 Hours	-	-	-	2/90/0	1/45/0
HT	SL	A 6	JEDEC JESD2 2-A103	1	45	High Temp Storage Bake 150C	20000 hrs.	-	-	1/45/0	2/90/0	1/45/0
							Test	Group B – Accelerated	Lifetime Simulation To	ests		
нт	OL	B 1	JEDEC JESD2 2-A108	3	77	Life Test, 125	1000 Hours	-	1/77/1 (Note 1)	3/231/0	3/231/0	-
ELI	FR	B 2	AEC Q100- 008	3	80 0	Early Life Failure Rate, 125C NVM	24 Hours	-	-	3/2400/0	-	-
ED	)R	B 3	AEC Q100- 005	3	77	Endurance, Data Retention, and Operational Life		N/A	N/A	N/A	N/A	N/A
							Tes	t Group C – Package A	ssembly Integrity Tes	ts		
WE	BS	C 1	AEC Q100- 001	1	30	Bond Shear (Cpk>1.67)	Wires	1/30/0	1/30/0	1/30/0	3/90/0	-
WE	BP	C 2	MIL- STD88 3 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	1/30/0	1/30/0	1/30/0	3/90/0	-
SI	D	C 3	JEDEC JESD2 2-B102	1	15	Surface Mount Solderability >95% Lead Coverage	8 Hours Steam Age	-	-	-	3/90/0	-
SI	D	C 3	JEDEC JESD2 2-B102	1	15	Surface Mount Solderability >95% Lead Coverage	8 Hours Steam Age	-	-	-	3/90/0	-
PI	D	C 4	JEDEC JESD2 2-B100 and B108	3	10	Physical Dimensions (Cpl->1.67)		-	-	3/90/0	3/90/0	-

		and B108									
		B108				Tes	t Group D – Die Fabrica	ation Reliability Tests			
EM	D 1	JESD61	-	-	Electromigrati on		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D 2	JESD35	-	-	Time Dependent Dielectric Breakdown		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D 3	JESD60 & 28	-	-	Hot Injection Carrier		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D 4	-	-	-	Negative Bias Temperature Instability		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D 5	-	-	-	Stress Migration		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
						T	est Group E – Electrica	l Verification Tests			
НВМ	E 2	AEC Q100- 002	1	3	ESD – HBM Pins RIN0+, RIN0-, RIN1+, RIN1-, RIN2+, RIN2-, RIN3+, RIN3-	6000 V	1/3/0	-	-	-	-
НВМ	E 2	AEC Q100- 002	1	3	ESD – HBM Other Pins	3000 V	1/3/0	-	1/3/0	1/3/0	1/3/0
НВМ	E 2	AEC Q100- 002	1	3	ESD – HBM Pins 32, 33, 41 and 42	8000 V	-	1/3/0	-	-	-
НВМ	E 2	AEC Q100- 002	1	3	ESD – HBM Other Pins	4500 V	-	1/3/0	-	-	-
CDM	E 3	AEC Q100- 011	1	3	ESD - CDM	1000 V	1/3/0	-	1/3/0	1/3/0	1/3/0
CDM	E 3	AEC Q100- 011	1	3	ESD - CDM	1250 V	-	1/3/0	-	-	-
LU	E 4	AEC Q100- 004	1	6	Latch-up	(Per AEC Q100- 004)	1/6/0	1/6/0	1/6/0	1/6/0	1/6/0
ED	E 5	AEC Q100- 009	3	30	Auto Electrical Distributions	Cpk>1.6 7	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level: Grade 0 (or E): -40°C to +150°C Grade 1 (or Q): -40°C to +125°C Grade 2 (or T): -40°C to +105°C Grade 3 (or I) : -40°C to +85°C

#### ${\bf E1\ (TEST):\ Electrical\ test\ temperatures\ of\ Qual\ samples\ (High\ temperature\ according\ to\ Grade\ level):}$

Room/Hot/Cold : HTOL, ED Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

#### Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

Note 1: 1 unit failed at the 1000 hour readpoint for leakage on a testpin and remained fully functional. Attributed to depressed wire that is not related to offload. FA and 8D attached to eQDB.

PCN 20210202001B.2 Texas Instruments, Inc.

# **Automotive New Product Qualification Summary**

(As per AEC-Q100 and JEDEC Guidelines)

# Approved 18-May-2021

#### **Product Attributes**

Attributes	Qual Device: DS90UB934TRGZRQ1	QBS Process Reference: DS90UB964TRGCRQ1	QBS Product and Package Reference: DS90UB934TRGZ
Automotive Grade Level	Grade 2	Grade 2	Grade 2
Operating Temp Range	-40 to +105 C	-40 to +105 C	-40 to +105 C
Wafer Fab Site	UMC-12A	UMC-12A	DMOS6
Die Revision	A0	A1	A0
Assembly Site	CLARK-AT	CLARK AT	CLARK-AT
Package Type	VQFN	VQFN	VQFN
Package Designator	RGZ	RGC	RGZ
Ball/Lead Count	48	64	48

### **Qualification Results**

Data Displayed as: Number of lots / Total sample size / Total failed

	Туре	#	Test Spec	Min Lot Qty	SS/ Lot	Test Name / Condition	Duration	Qual Device: DS90UB934TRGZRQ 1	QBS Process and Package Reference: DS90UB964TRGCRQ1	QBS Product Reference: DS90UB934TRGZ
						Test Gr	oup A – Acce	lerated Environment Stress	Tests	
	PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Automotive Preconditioning	Level 3- 260C	-	3/Pass	1/Pass
	HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST, 110C/85%RH	528 Hours	-	3/231/0	-
	HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST, 130C/85%RH	96 Hours	-	-	1/77/0
	HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST, 130C/85%RH	192 Hours	-	-	-
	AC	A3	JEDEC JESD22- A102	3	77	Autoclave 121C	192 Hours	-	-	
1	UHAST	A3	JEDEC JESD22- A118	3	77	Unbiased HAST, 110C/85%RH	264 Hours	-	3/231/0	-
1	UHAST	A3	JEDEC JESD22- A118	3	77	Unbiased HAST, 130C/85%RH	96 Hours	-	-	1/77/0
	TC	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	-	3/231/0	1/77/0
	TC	A4	JEDEC JESD22- A104 and Appendix	3	77	Temperature Cycle, -65/150C	1000 Cycles	-	3/219/0	-
	TC-BP	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Post Temp. Cycle, Bond Pull	Wires	-	1/30/0	-
	PTC	A5	JEDEC JESD22- A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	NA	N/A
	HTSL	A6	JEDEC JESD22- A103	1	45	High Temp Storage Bake 150C	500 Hours	-	-	1/45/0
	HTSL	A6	JEDEC JESD22- A103	1	45	High Temp Storage Bake 150C	1000 Hours	-	1/45/0	

<sup>-</sup> QBS: Qual By Similarity - Qual Devices qualified at LEVEL3-260C: DS90UB934TRGZRQ1

Test Group B – Accelerated Lifetime Simulation Tests										
HTOL	В1	JEDEC JESD22- A108	3	77	Life Test, 125	1000 Hours	-	3/231/0	3/231/0	
ELFR	B2	AEC Q100- 008	3	80 0	Early Life Failure Rate, 125C	24 Hours	-	3/2400/0	-	
EDR	В3	AEC Q100- 005	3	77	NVM Endurance, Data Retention, and Operational Life		N/A	N/A	N/A	
					Test (	Group C – Pa	ckage Assembly Integrity T	ests		
WBS	C1	AEC Q100- 001	1	30	Bond Shear (Cpk>1.67)	Wires	1/30/0	1/30/0	-	
WBP	C2	MIL- STD883 Method 2011	1	30	Bond Pull (Cpk>1.67)	Wires	1/30/0	1/30/0	-	
SD	СЗ	JEDEC JESD22- B102	1	15	Surface Mount Solderability >95% Lead Coverage	8 Hours Steam Age	-	-	-	
SD	C3	JEDEC JESD22- B102	1	15	Surface Mount Solderability >95% Lead Coverage	8 Hours Steam Age	-	-	-	
PD	C4	JEDEC JESD22- B100 and B108	3	10	Physical Dimensions (Cpk>1.67)		-	3/90/0	-	
Test Group D – Die Fabrication Reliability Tests										
					Test	Group D - D				
EM	D1	JESD61	-	-	Electromigration		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	
EM TDDB	D1	JESD61 JESD35	-	-			Completed Per Process Technology	Completed Per Process Technology		
				-	Electromigration  Time Dependant Dielectric		Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology	Requirements  Completed Per Process Technology	
TDDB	D2	JESD35 JESD60		-	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection		Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements Completed Per Process Technology Requirements Completed Per Process Technology	Requirements  Completed Per Process Technology Requirements  Completed Per Process Technology	
TDDB HCI	D2	JESD35  JESD60 & 28	-	-	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Requirements  Completed Per Process Technology Requirements  Completed Per Process Technology Requirements  Completed Per Process Technology	
TDDB  HCI  NBTI	D2 D3 D4	JESD35  JESD60 & 28	-	-	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration		Completed Per Process Technology Requirements Completed Per Process Technology	Completed Per Process Technology Requirements	Requirements  Completed Per Process Technology Requirements	
TDDB  HCI  NBTI	D2 D3 D4	JESD35  JESD60 & 28	-	-	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration		Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Requirements  Completed Per Process Technology Requirements	
TDDB  HCI  NBTI  SM	D2 D3 D4 D5	JESD35  JESD60 & 28  AEC Q100-	-	-	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration	   st Group E –	Completed Per Process Technology Requirements Electrical Verification Test	Completed Per Process Technology Requirements	Requirements  Completed Per Process Technology Requirements	
TDDB  HCI  NBTI  SM  HBM	D2 D3 D4 D5 E2	JESD35  JESD60 & 28  -  -  AEC Q100- 002  AEC Q100-	1	3	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration  Te  ESD - HBM	  st Group E – 2000 V	Completed Per Process Technology Requirements Electrical Verification Test	Completed Per Process Technology Requirements Sompleted Per Process Technology Requirements	Requirements  Completed Per Process Technology Requirements  1/3/0	
TDDB  HCI  NBTI  SM  HBM  CDM	D2 D3 D4 D5 E2 E3	JESD35  JESD60 & 28  -  -  AEC Q100- 002  AEC Q100- 011  AEC Q100-	1	3	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration  Te  ESD - HBM	st Group E – 2000 V 750 V (Per AEC Q100-	Completed Per Process Technology Requirements Electrical Verification Test 1/3/0	Completed Per Process Technology Requirements S 1/3/0	Requirements  Completed Per Process Technology Requirements  1/3/0  1/3/0	
TDDB  HCI  NBTI  SM  HBM  CDM  LU	D2 D3 D4 D5 E2 E3 E4 E4 E5	JESD35  JESD60 & 28		- - - 3 3 6 6	Electromigration  Time Dependant Dielectric Breakdown  Hot Injection Carrier  Negative Bias Temperature Instability  Stress Migration  Te  ESD - HBM  ESD - CDM  Latch-up, 25C	st Group E 2000 V  750 V  (Per AEC Q100-004) (Per AEC Q100-	Completed Per Process Technology Requirements Lectrical Verification Test 1/3/0 1/3/0	Completed Per Process Technology Requirements  1/3/0  1/3/0	Requirements  Completed Per Process Technology Requirements  1/3/0  1/3/0  1/6/0	

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

**Ambient Operating Temperature by Automotive Grade Level:** 

Grade 0 (or E): -40°C to +150°C Grade 1 (or Q): -40°C to +125°C Grade 2 (or T): -40°C to +105°C Grade 3 (or I): -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

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PCN 20210202001B.2 Texas Instruments, Inc.

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