

SP5002 6 Channel Common Mode Filter



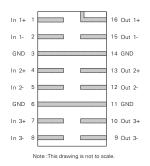


Description

The SP5002 Series is a highly integrated Common Mode Filter (CMF) providing both ESD protection and EMI common mode noise filtering for systems using high speed differential serial interfaces, such as MIPI D-PHY.

The SP5002 Series can protect and filter three differential line pairs in a small RoHS-compliant TDFN-16 package, with cost and space savings over discrete solutions.

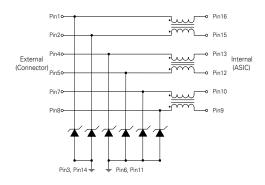
Pinout



Features

- Large differential bandwidth > 2GHz
- High Common Mode Stop Band Attenuation:
 - > 25 dB at 700 MHz > 30 dB at 800 MHz
- ±15kV ESD protection per channel (IEC 61000-4-2 Level 4, contact discharge and ±30kV air discharge)
- TDFN-16 4.00mm × 2.00mm × 0.75mm package with 0.50mm lead pitch
- RoHS-compliant, Leadfree packaging
- AEC-Q101 qualified
- Moisture Sensitivity Level (MSL-1)

Functional Block Diagram



Applications

- MIPI D-PHY (CSI-2, DSI, etc) in Mobile Phones and Digital Still Cameras
- HDMI/DVI Display in Mobile Phones

Absolute Maximum Ratings

Symbol	Parameter Value		Units
I _{DC}	DC Current Per Line	100	mA
P _{DC}	DC Package Power Rating	0.5	W
T _{OP}	Operating Temperature	-40 to 125	°C
T _{STOR}	Storage Temperature	-55 to 150	°C

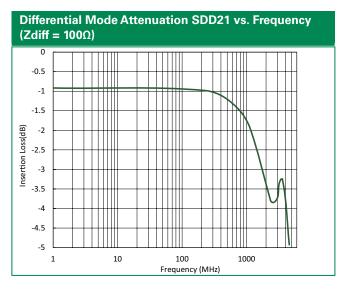
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the component. This is a stress only rating and operation of the component at these or any other conditions above those indicated in the operational sections of this specification is not implied.

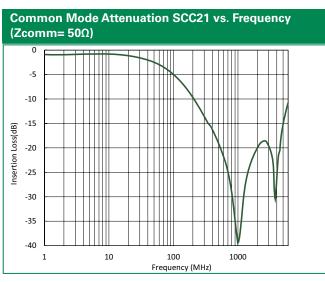
Electrical Characteristics (T_{OP}=25°C)

Parameter	Symbol	Test Conditions	Min	Тур	Max	Units
Channel Resistance	R _{CH}	Pins 1–10, 2–9, 4–7 and 5–6		8.0		Ω
Total Channel Capacitance	C _{TOTAL}	$V_{I/O} = 1.65V_{DC}$ Reverse Bias; f=1MHz, 30mV _{AC}		0.8	1.3	pF
Reverse Standoff Voltage	V _{RWM}				5.0	V
Breakdown Voltage	V _{BR}	I _T =1mA	6.0	8.0	10.0	V
Forward Voltage at I _F	V _F	I _F =1mA	0.4	0.7	1.5	V
Reverse Leakage Current	I _{LEAK}	V _{VO} =3.3V		0.01	0.10	μΑ
	R _{DYN}	Positive (tp=8/20µs)		1.3		
Dynamic Resistance ^{2 3}		Negative (tp=8/20µs)		0.7		Ω
		TLP, tp=100ns, I/O to GND		0.36		
ESD Withstand Voltage ¹²	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	IEC 61000-4-2 (Contact Discharge)	±15			kV
L3D Withstand Voltage	V _{ESD}	IEC 61000-4-2 (Air Discharge)	±30			kV
Differential Mode Cutoff Frequency ²	F _{3dB}	Z_{SOURCE} =50 Ω , Z_{LOAD} 50 Ω		2.0		GHz
Common Mode Stop Band Attenuation ²	F _α	f=800MHz		30		dB

Notes: $^{\mbox{\tiny 1}}$ ESD zapping at I/O pins (1,2,4,5,7,8) with respect to GND.

³ Transmission Line Pulse (TLP) with 100ns width and 200ps rise time.

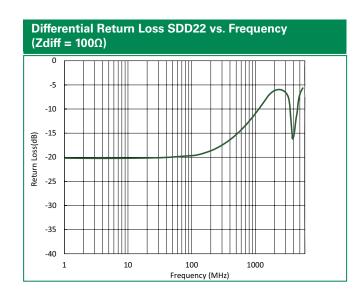




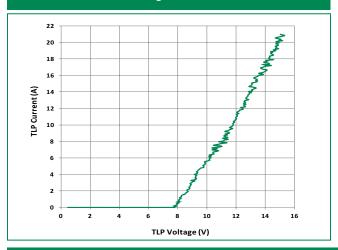
² Guaranteed by design.



Differential Return Loss SDD11 vs. Frequency (Zdiff = 100Ω) -5 -10 -10 -15 -20 -20 -35 -40 1 10 100 1000 Frequency (MHz)

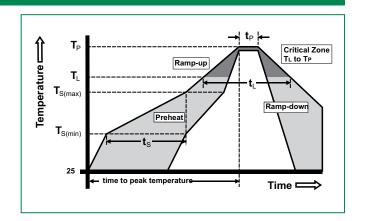


Transmission Line Pulsing (TLP) Plot



Soldering Parameters

Reflow Cor	ndition	Pb – Free assembly	
Pre Heat	-Temperature Min (T _{s(min)})	150°C	
	-Temperature Max (T _{s(max)})	200°C	
	-Time (min to max) (t _s)	60 – 180 secs	
Average rai	verage ramp up rate (Liquidus) Temp (T _L) 3°C/second ma		
T _{S(max)} to T _L	- Ramp-up Rate	3°C/second max	
Reflow	-Temperature (T _L) (Liquidus)	217°C	
nellow	-Temperature (t _L)	60 – 150 seconds	
Peak Tempe	erature (T _P)	260 ^{+0/-5} °C	
Time within 5°C of actual peak Temperature (t _p)		20 - 40 seconds	
Ramp-down Rate		6°C/second max	
Time 25°C	to peak Temperature (T _P)	8 minutes Max.	
Do not exceed		260°C	



Product Characteristics

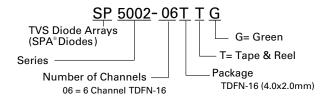
Lead Plating	Pre-Plated Frame		
Lead Material	Copper Alloy		
Substrate material	Silicon		
Body Material	V-0 per UL 94 Molded Epoxy		

Ordering Information					
Part Number	Package	Size	Marking	Min. Order Qty.	
SP5002-06TTG	TDFN-16	4.0x2.0mm	C33****	3000	

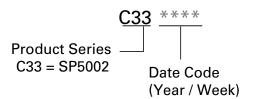
Notes:

- 1. All dimensions are in millimeters
- 2. Dimensions include solder plating.
- 3. Dimensions are exclusive of mold flash & metal burr.
- 4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
- 5. Package surface matte finish VDI 11-13.

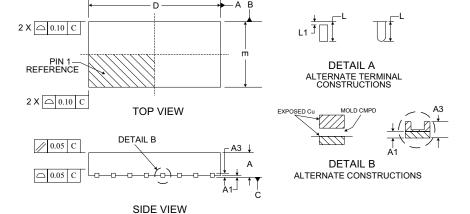
Part Numbering System



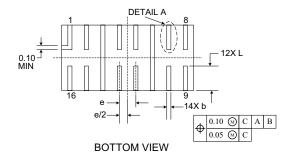
Part Marking System

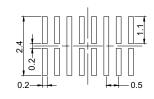


Package Dimensions — TDFN-16



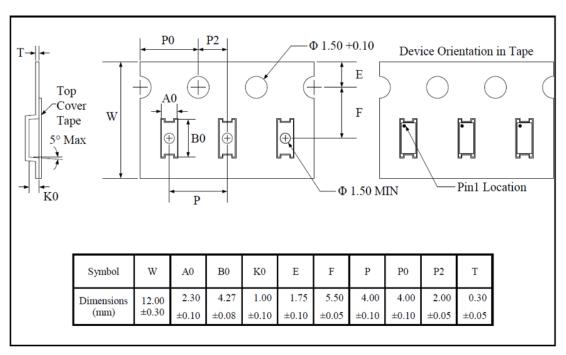
		TDFN-16				
		JEDEC MO-229				
	Millin	neters	Inches			
	Min	Max	Min	Max		
Α	0.70	0.80	0.028	0.031		
A 1	0.00	0.05	0.00	0.002		
А3	0.20 REF		0.008 REF			
b	0.15	0.25	0.006	0.010		
D	3.95	4.05	0.156	0.159		
E	1.95	2.05	0.077	0.081		
е	0.50 BSC		0.020 BSC			
L	0.70	0.90	0.028	0.035		
L1	0.05	0.15	0.002	0.006		

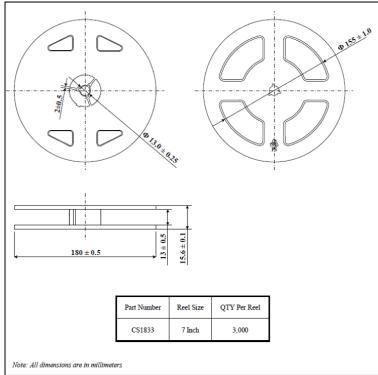




TDFN-16 Soldering Pattern RECOMMENDED SOLDER PAD LAYOUT

Tape and Reel Specifications





Disclaimer Notice - Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at www.littelfuse.com/disclaimer-electronics.