Keywords: framer, single chip transceivers, SCTs, T1, E1, initialization, programming

APPLICATION NOTE 342

T1/E1 Framer Initialization and Programming

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Abstract: This application note highlights the initialization and programming of Maxim framers.

Introduction

This application note shows how to initialize and program Maxim T1/E1 framers. The DS2155, DS21Q55, and DS2156 do not require any special initialization after power-up, since they automatically initialize themselves by clearing and setting the proper registers.

General Initialization

After power-up, when supplies and clocks have stabilized, internal registers must be initialized. Please note the DS2155, DS21Q55, and DS2156 do NOT require any special initialization whatsoever since they automatically initialize upon power-up. It is a good idea to clearµset to 0x00µALL R/W registers. The easiest way to do this is to write 0x00 to address space 0x00-0xFF, regardless of register type. Certain registers have bits that control special test modes and features that can provide confusing indications (Table 1).

Table 1. Registers with Special Test Modes and Features

Part	Name
DS2151	TEST, TCR2, LICR
DS2152	TEST1, TEST2, TCR2, LICR
DS21352/552	TEST1, TEST2, TCR2, LICR
DS21Q41/Q42	TEST, TCR2
DS21FF/FT42	TEST1, TCR2
DS2153	TEST1, TEST2, LICR
DS2154	TEST1, TEST2, LICR
DS21354/554	TEST1, TEST2, TCR2, LICR
DS21Q43/Q44	TEST1, TEST2
DS21FF/FT44	TEST1, TEST2

Depending on the interrupt structure implemented, it may be a good idea to clear IMR1 and IMR2 first. Prior to clearing these two registers, spurious interrupt signals may occur without an external interrupt disable.

Once the registers have been initialized and set up with the transceiver's mode of operation, the line interface reset bit should be set high, then low. If the elastic store is enabled, the ESR bit should be set, then cleared.

Special Initialization for DS2141

Transmit clock (TCLK) must be present for proper port initialization. Network signals (loop timing) cannot be guaranteed to replace a missing TCLK during initialization. The following sequence should be used to initialize the DS2141, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Write 0x00 to all other R/W registers
2. Write initial device configuration data
3. Wait for SYSCLK to stabilize if elastic stores enabled

Special Initialization for DS21Q41

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the DS21Q41, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in TCR1 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
6. Set ESR bit in CCR3 register if elastic stores enabled
7. Clear ESR bit

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in TCR1 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS21Q42

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the DS21Q42, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in TCR1 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
6. Set TESR and RESR bits in CCR7 register if elastic stores enabled
7. Clear TESR and RESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in TCR1 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS2143

Transmit clock (TCLK) must be present for proper port initialization. Network signals (loop timing) cannot be guaranteed to replace a missing TCLK during initialization. The following sequence should be used to initialize the DS2143, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Write 0x00 to all other R/W registers
2. Write initial device configuration data
3. Wait for SYSCLK to stabilize if elastic stores enabled

Special Initialization for DS21Q43

Transmit Clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK via the LOSS of TRANSMIT CLOCK mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the DS21Q43 in which TCLK is not present or TCLK is derived from RCLK (a loop timed system).

1. Set LOTCMC bit in CCR2 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Wait for TSYSCLK and RSYSCLK to stabilize (if elastic store(s) enabled)
6. Set ESR bit in CCR3 register (if elastic store(s) enabled)
7. Clear ESR bit

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in CCR2 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS21Q44

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the DS21Q44, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in CCR2 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Wait for TSYSCLK and RSYSCLK to stabilize (if elastic store(s) enabled)
6. Set TESR and RESR bits in CCR6 register (if elastic store(s) enabled)
7. Clear TESR and RESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in CCR2 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS2151

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled

by setting TCR1.7. The following sequence should be used to initialize the DS2151, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in TCR1 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. SET LIRST bit in CCR3 register
6. Wait for SYSCLK to stabilize if elastic stores enabled
7. Set ESR bit in CCR3 register if elastic stores enabled
8. Clear LIRST and ESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in TCR1 be enabled.
Note 2: If the SYSCLK pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS2152

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the DS2152, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in TCR1 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Set LIRST bit in CCR7 register
6. Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
7. Set ESR bit in CCR3 register if elastic stores enabled
8. Clear LIRST and ESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in TCR1 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS2153

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the DS2153, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in CCR2 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Set LIRST bit in CCR3 register
6. Wait for SYSCLK to stabilize (if elastic store(s) enabled)
7. Set ESR bit in CCR3 register (if elastic store(s) enabled)
8. Clear LIRST and ESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is

recommended that LOTCMC in CCR2 be enabled.
Note 2: If the SYSCLK pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS2154

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the DS2154, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in CCR2 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Set LIRST bit in CCR5 register
6. Wait for TSYSCLK and RSYSCLK to stabilize (if elastic store(s) enabled)
7. Set ESR bit in CCR3 register (if elastic store(s) enabled)
8. Clear LIRST and ESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in CCR2 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS21FF/FT42

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the DS21FF/FT42, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in TCR1 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Wait for SYSCLK to stabilize if elastic stores enabled
6. Set TESR and RESR bits in CCR7 register if elastic stores enabled
7. Clear TESR and RESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in TCR1 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS21FF/FT44

Transmit Clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the DS21FF/FT44, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in CCR2 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data

5. Wait for SYSCLK to stabilize if elastic stores enabled
6. Set TESR and RESR bits in CCR6 register if elastic stores enabled
7. Clear TESR and RESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in CCR2 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS21x52

Transmit clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting TCR1.7. The following sequence should be used to initialize the DS21x52, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in TCR1 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Set LIRST bit in CCR7 register
6. Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
7. Set TESR and RESR bits in CCR7 register high if elastic stores enabled
8. Clear LIRST, TESR, and RESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in TCR1 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Special Initialization for DS21x54

Transmit Clock (TCLK) must be present for proper port initialization. This clock can be sourced externally from the TCLK pin or internally from RCLK through the loss-of-transmit clock mux. This mux is enabled by setting CCR2.2. The following sequence should be used to initialize the DS21x54, in which TCLK is not present or TCLK is derived from RCLK (a loop-timed system).

1. Set LOTCMC bit in CCR2 register
2. Wait 10ms minimum
3. Write 0x00 to all other R/W registers
4. Write initial device configuration data
5. Set LIRST bit in CCR5 register
6. Wait for TSYSCLK and RSYSCLK to stabilize if elastic stores enabled
7. Set TESR and RESR bits in CCR6 register high if elastic stores enabled
8. Clear LIRST, TESR, and RESR bits

Note 1: In loop-timed configurations, or when TCLK is not guaranteed to always be present, it is recommended that LOTCMC in CCR2 be enabled.
Note 2: If the TEST pin is high, registers can be written to (initialized), but not read.

Conclusion

If you have further questions about T1/E1 framer initialization and programming, please contact the Telecommunication Applications support team.

T1/E1 Framer Information

For more information about our T1/E1 framers, please consult the respective data sheets available on our website at www.maximintegrated.com/telecom.

Related Parts		
DS21352	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS2152	Enhanced T1 Single Chip Transceiver	
DS2154	Enhanced E1 Single Chip Transceiver	
DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS21FF42	4 x 4 16 Channel T1 Framer / 4 x 3 12 Channel T1 Framer	
DS21FF44	4x3 Twelve Channel E1 Framer / 4x4 Sixteen Channel E1 Framer	
DS21FT42	4 x 4 16 Channel T1 Framer / 4 x 3 12 Channel T1 Framer	
DS21FT44	4x3 Twelve Channel E1 Framer / 4x4 Sixteen Channel E1 Framer	Free Samples
DS21Q42	Enhanced Quad T1 Framer	
DS21Q44	Enhanced Quad E1 Framer	

More Information
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Application Note 342: http://www.maximintegrated.com/an342
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